

# 915GV-M5A

Rev: 1.0B

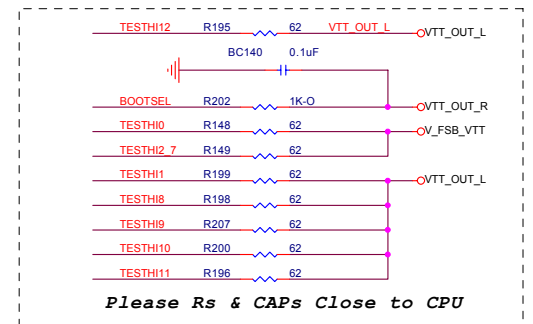
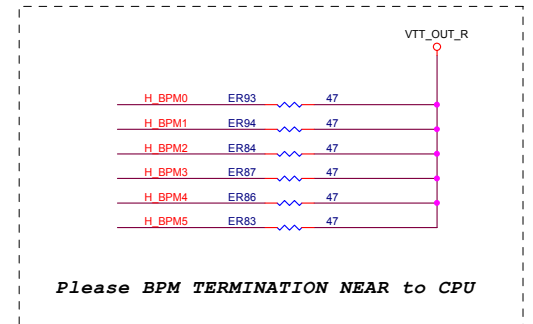
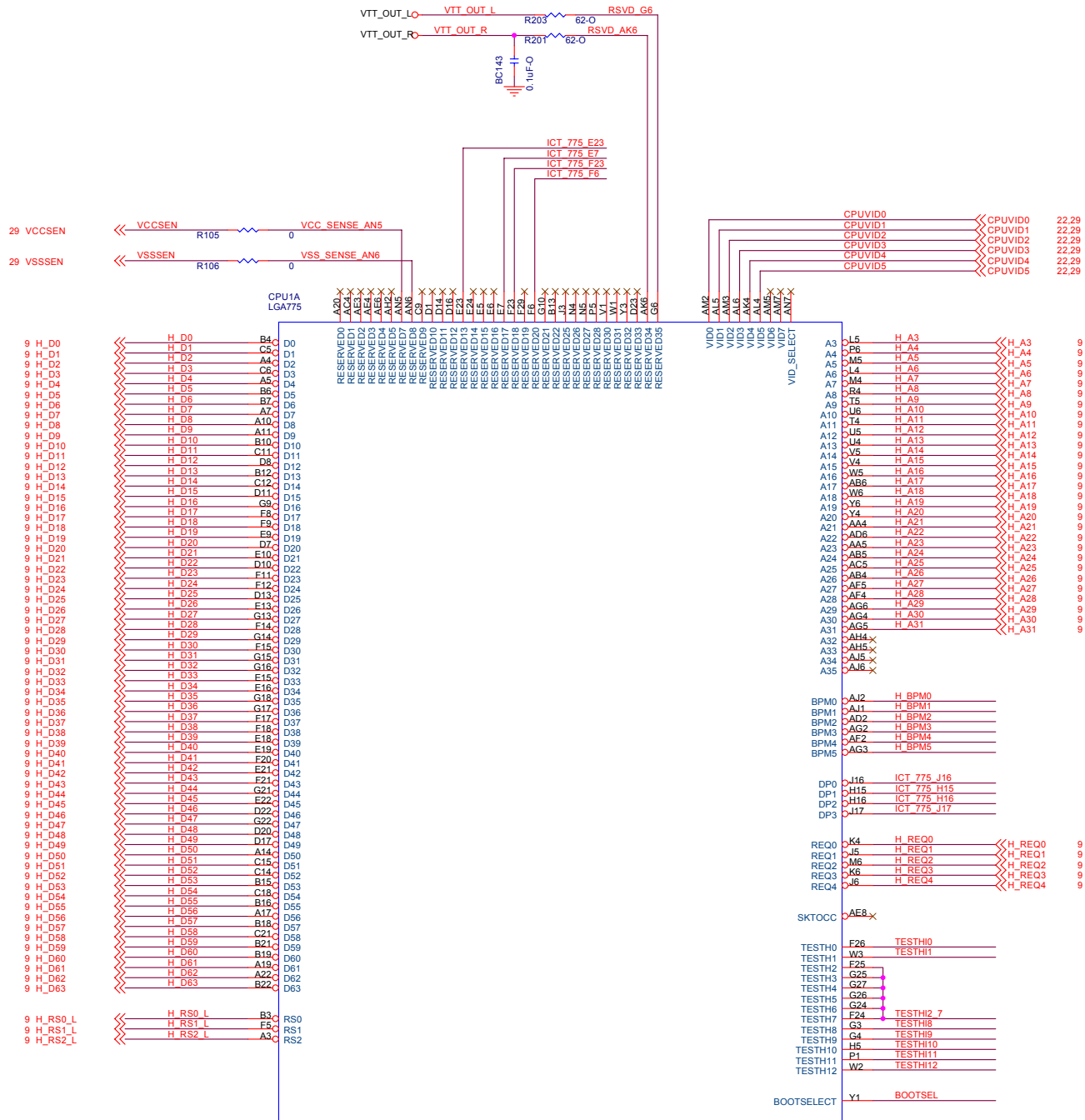
Page Title of Schematic :

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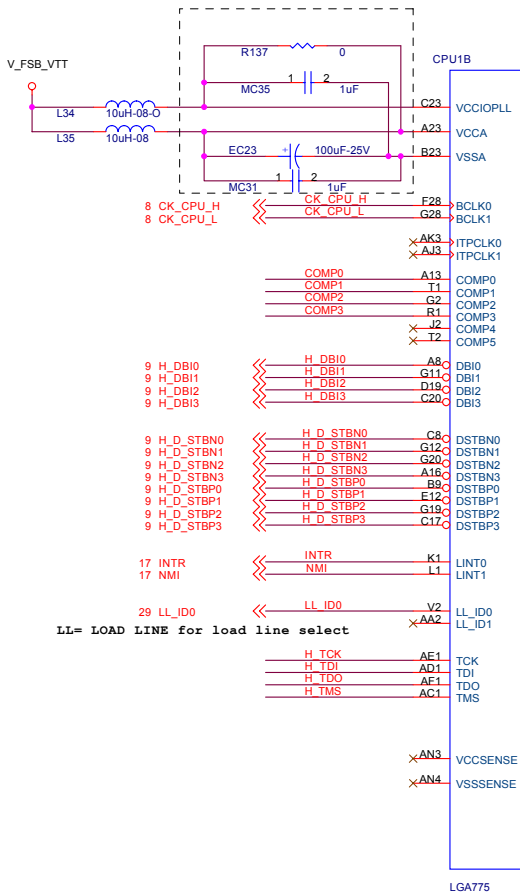
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C	C	36	28,29,33	09/20/' 04
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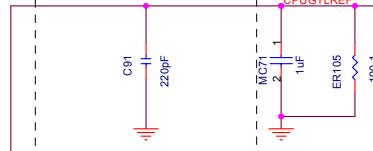




Place componets as close as possible to Processor socket  
trace width to cap must be no smaller than 12 Mils

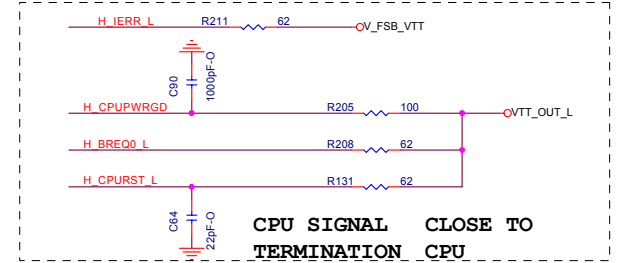


Close CPU H1 pin



$$GTLREF = 0.67 * VTT = 0.8V$$

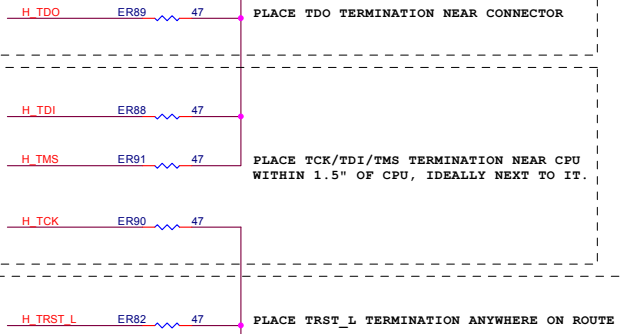
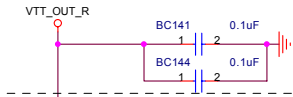
GTLREF GENERATION CIRCUITS



CPU SIGNAL CLOSE TO TERMINATION CPU



BSEL resistors can be removed IF ONLY TEJAS AND CEDAR MILL ARE SUPPORTED

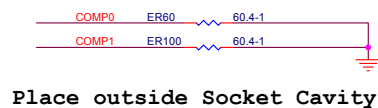


PLACE TDO TERMINATION NEAR CONNECTOR

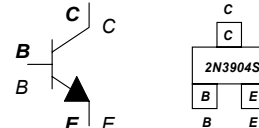
PLACE TCK/TDI/TMS TERMINATION NEAR CPU WITHIN 1.5" OF CPU, IDEALLY NEXT TO IT.

PLACE TRST\_L TERMINATION ANYWHERE ON ROUTE

Layout need closed CPU



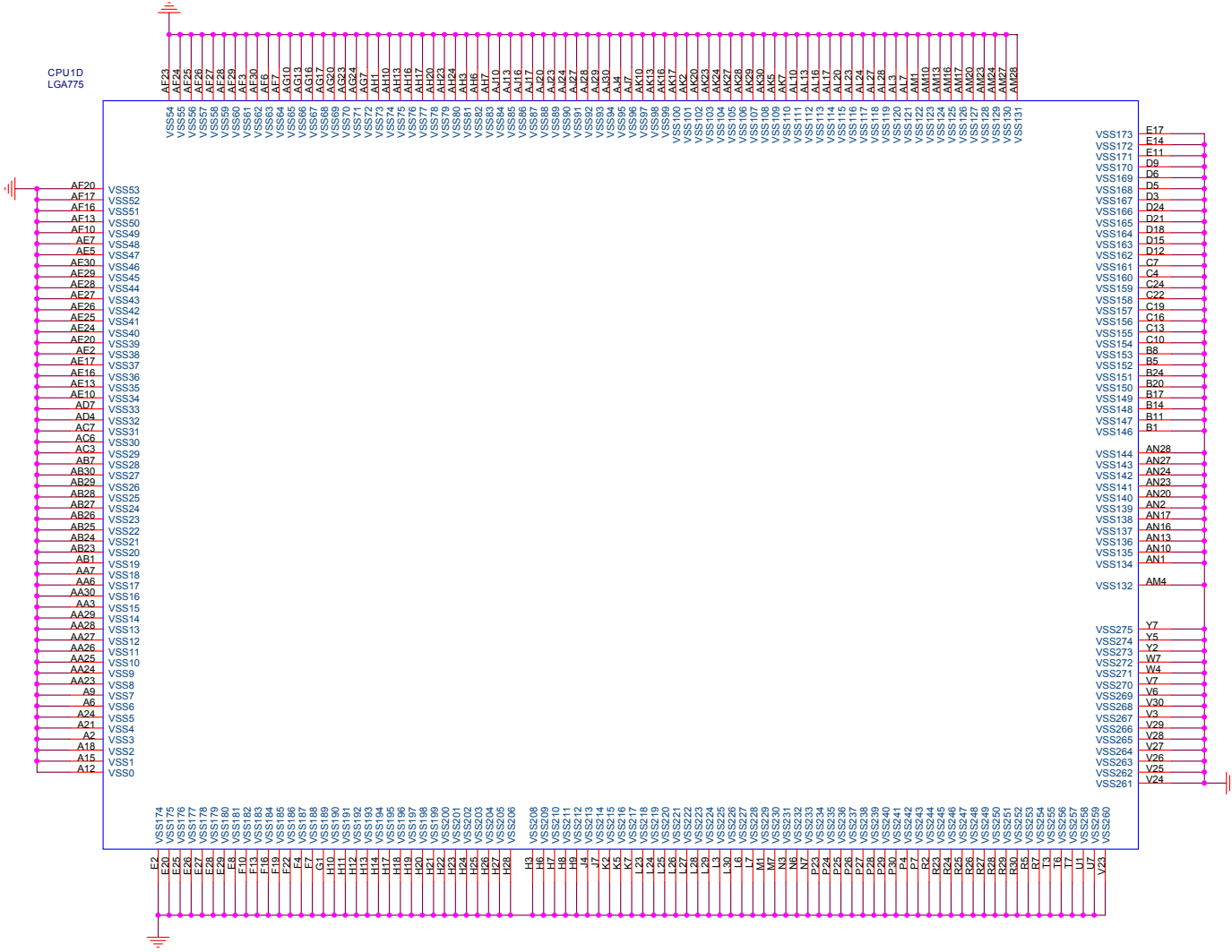
Place outside Socket Cavity

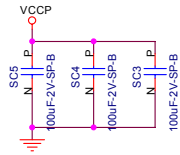
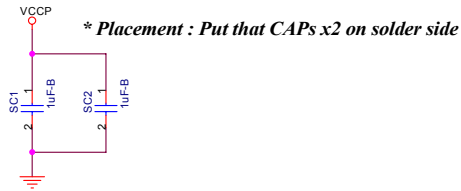
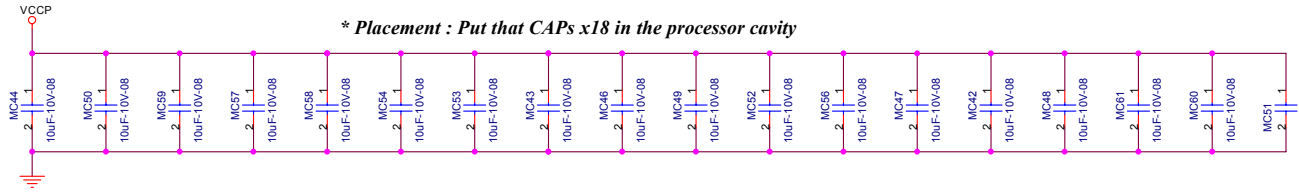




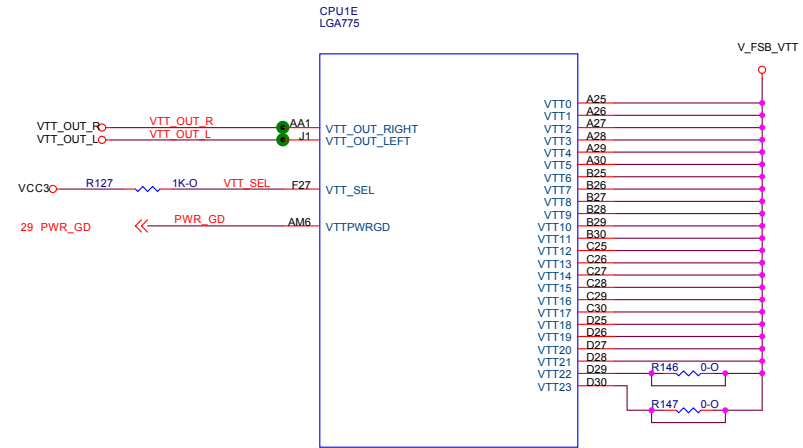
CPU1C  
LGA775

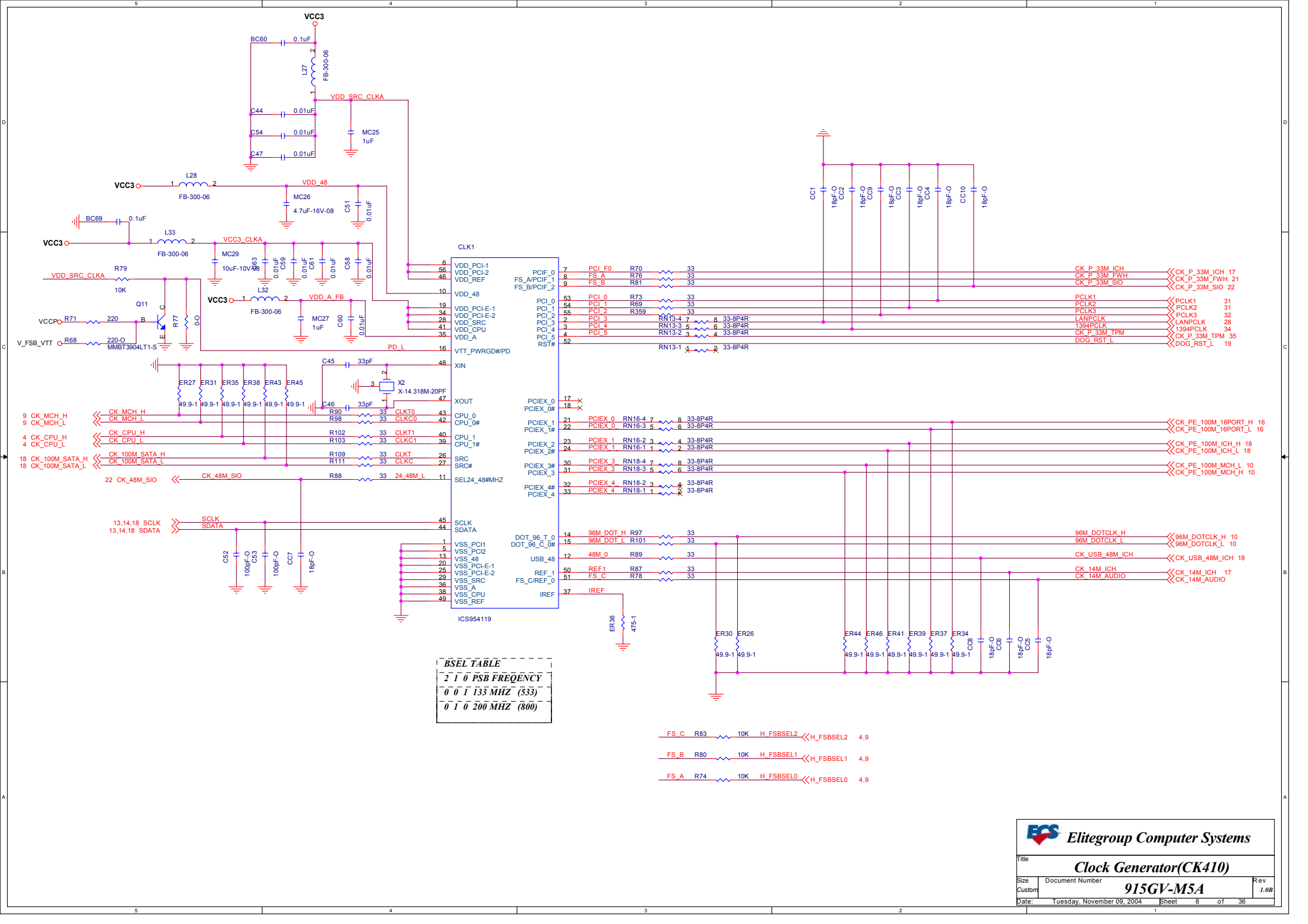
CPU1D  
LGA775





VTT\_SEL=0 for the Tejas processor

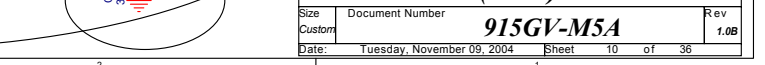
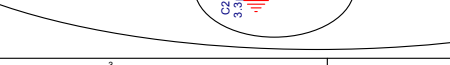
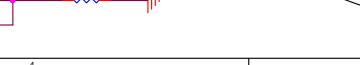
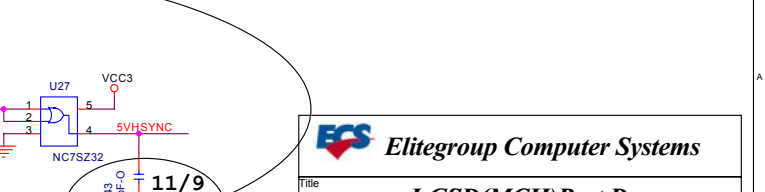
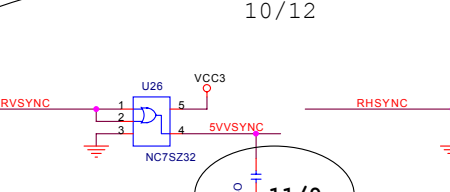
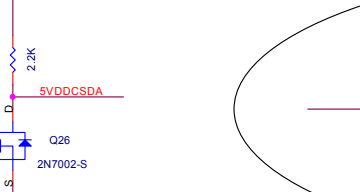
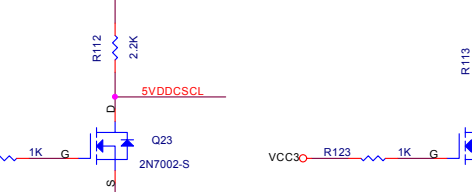
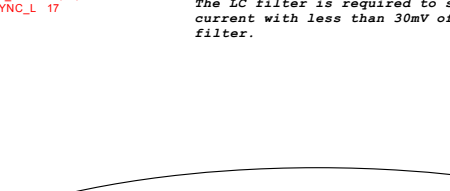
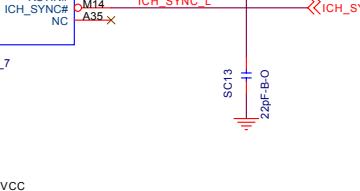
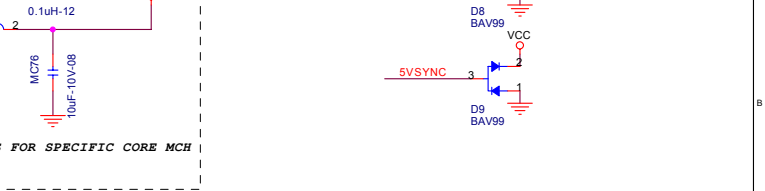
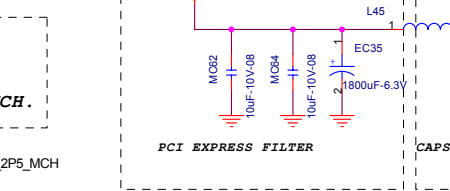
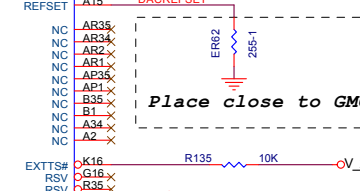
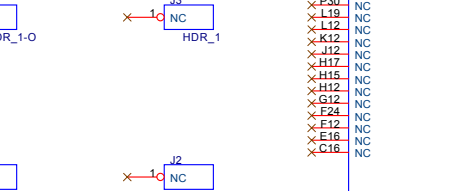
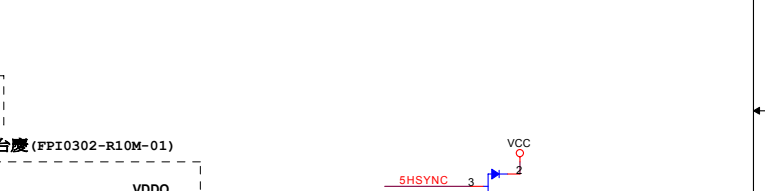
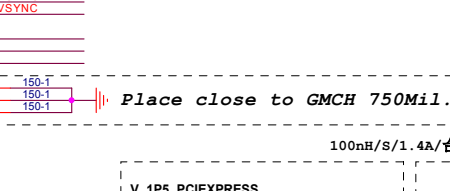
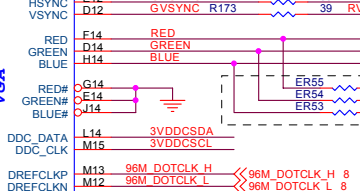
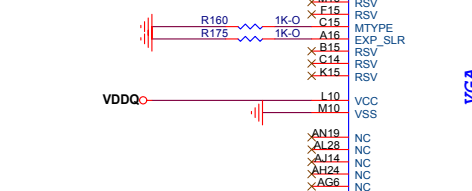
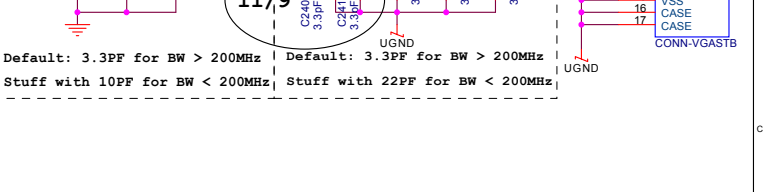
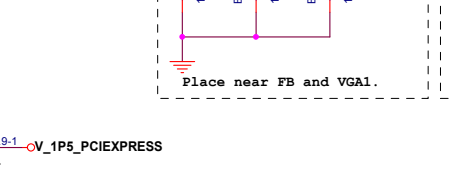
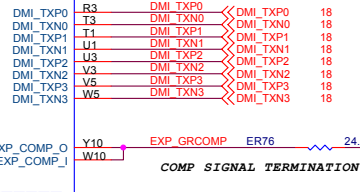
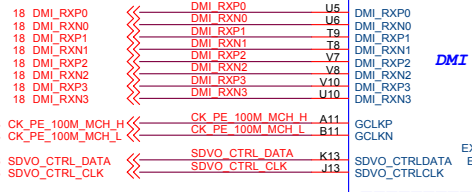
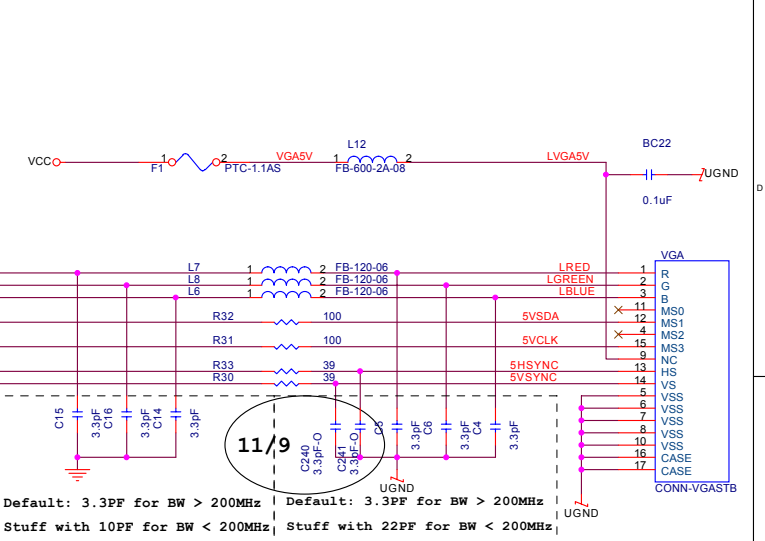
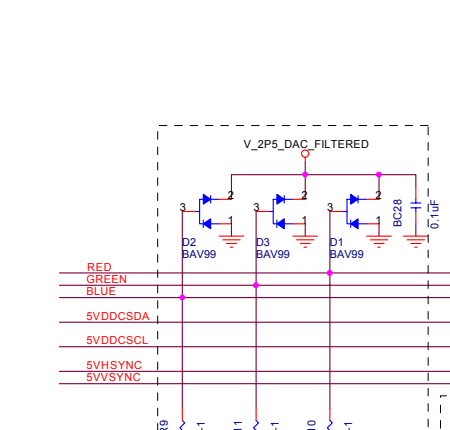
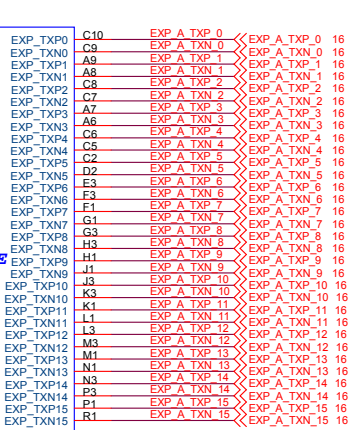
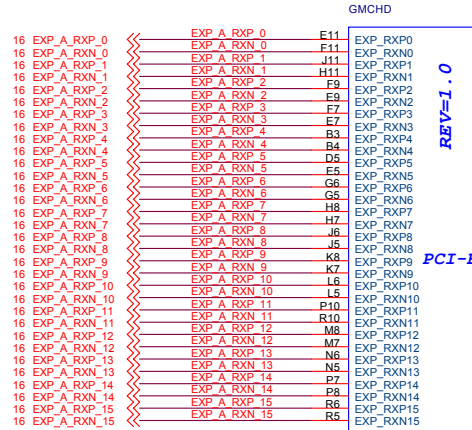


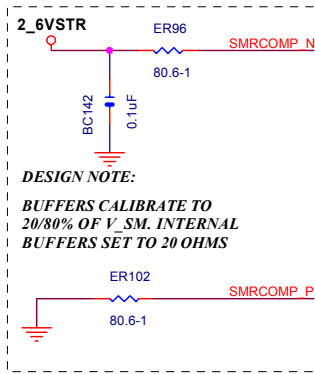



BSEL TABLE		
2	1	0 PSB FREQUENCY
0	0	1 133 MHZ (533)
0	1	0 200 MHZ (800)

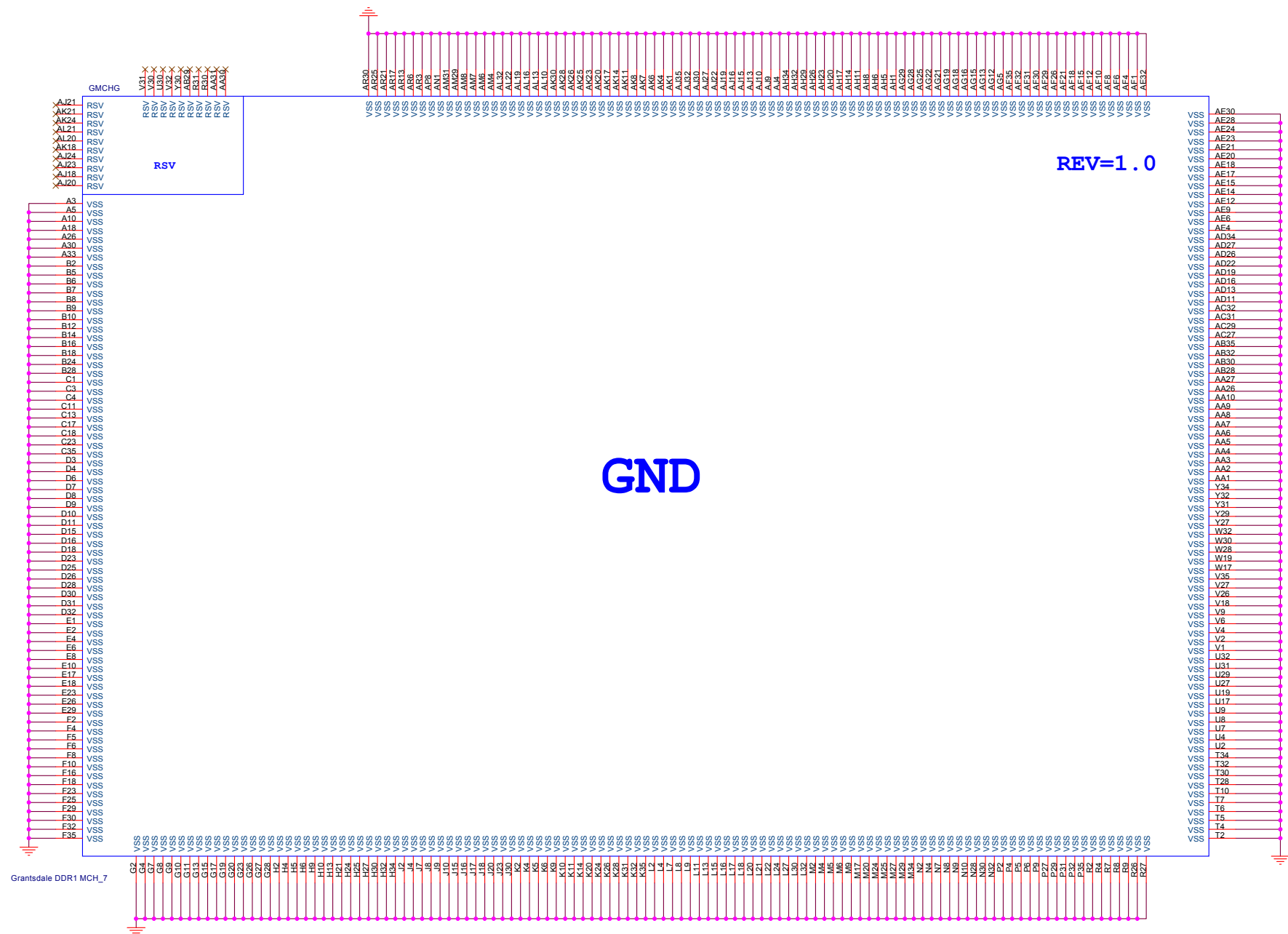


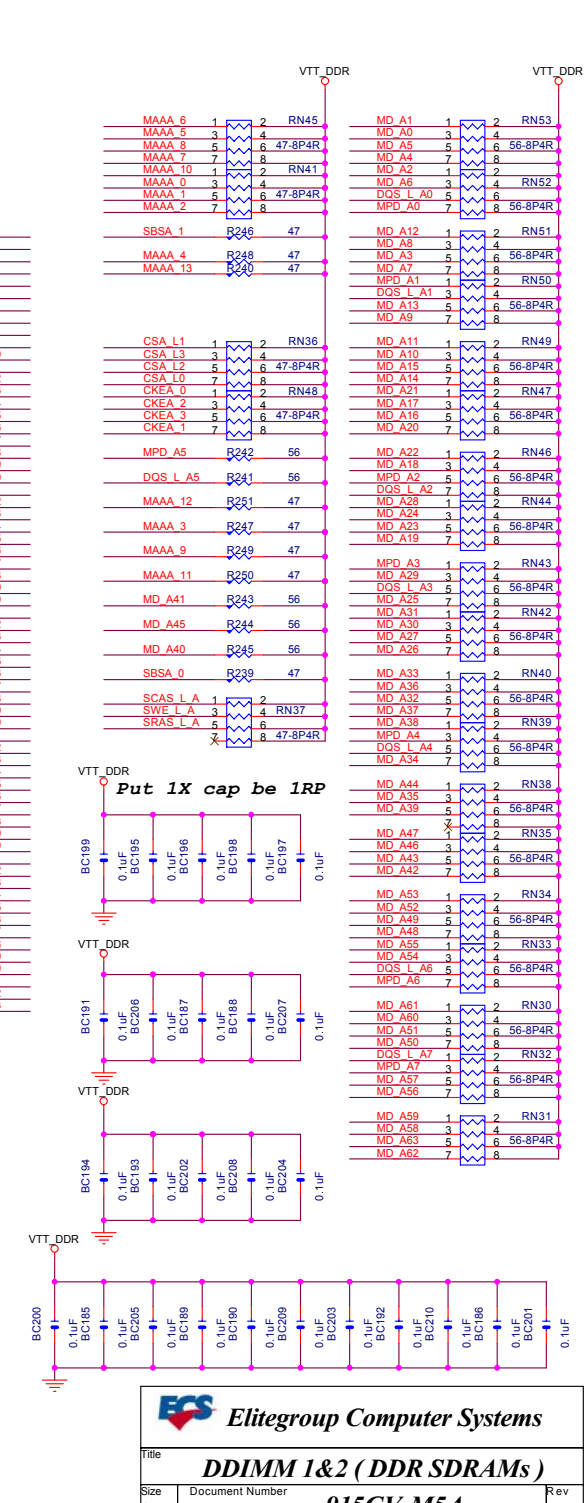
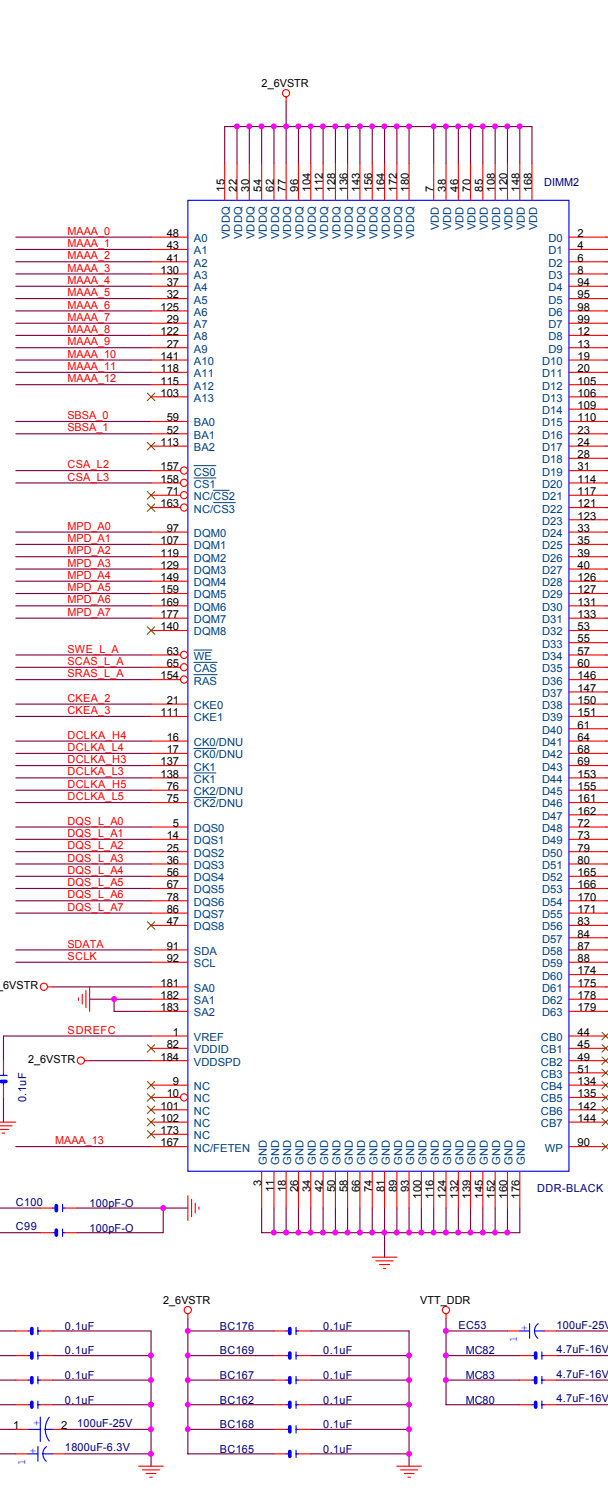
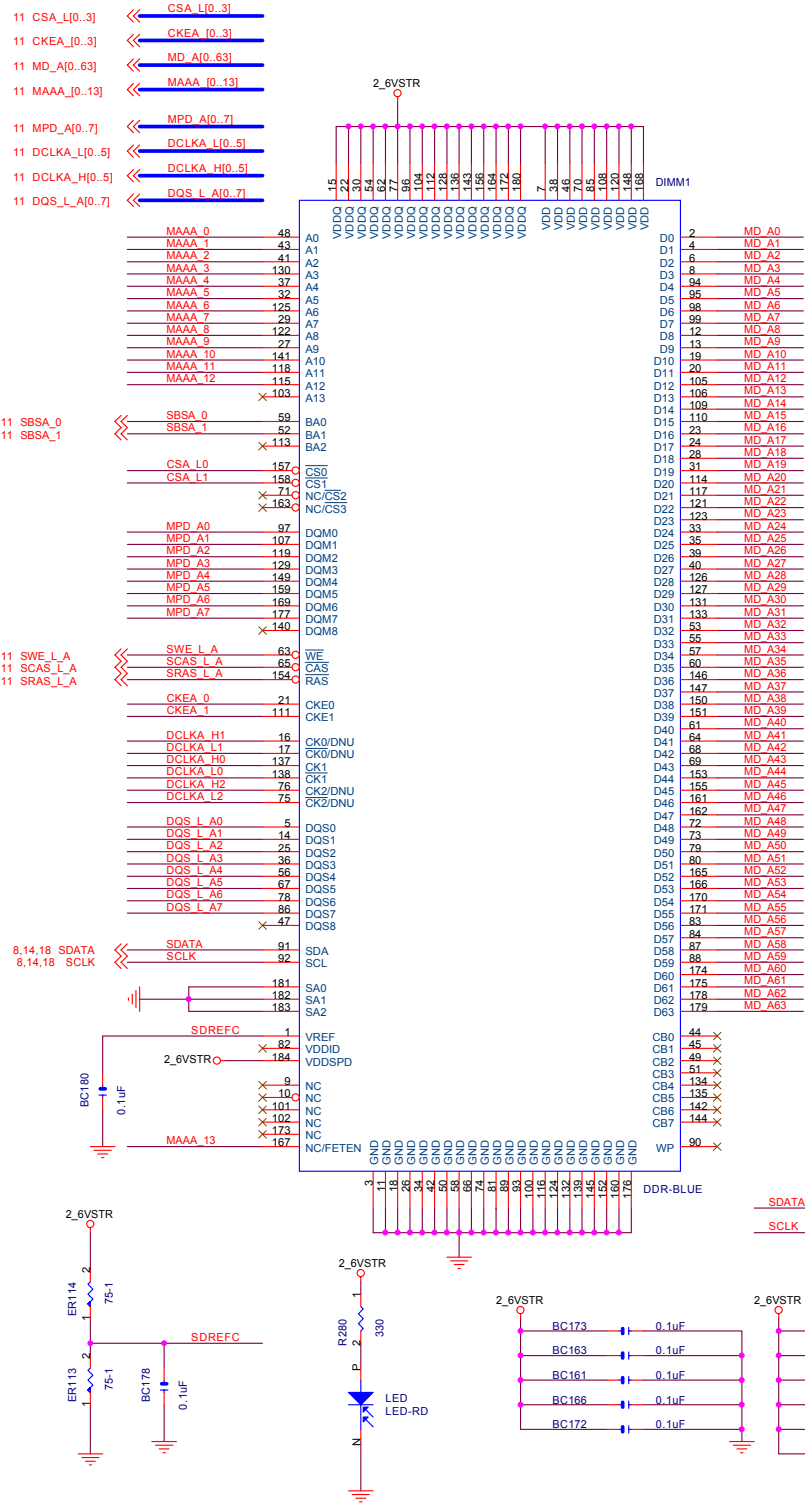




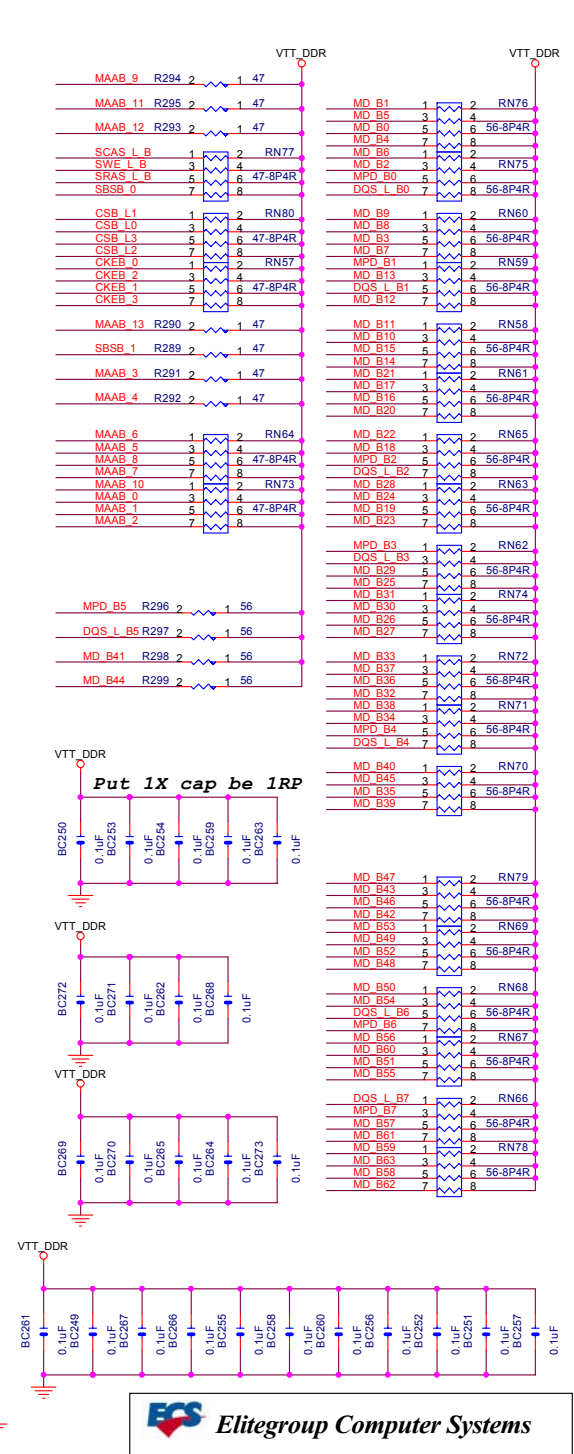


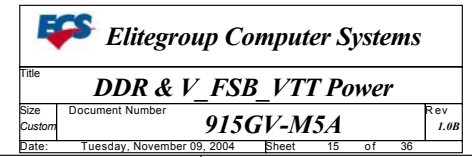
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<b>Title</b> <b><i>I-GSD(MCH)Part B &amp; C</i></b>			
<b>Size</b> <b>B</b>	<b>Document Number</b> <b><i>915GV-M5A</i></b>		<b>Rev</b> <b><i>1.0B</i></b>
<b>Date:</b> Tuesday, November 09, 2004		<b>Sheet</b> 11 <b>of</b> 36	





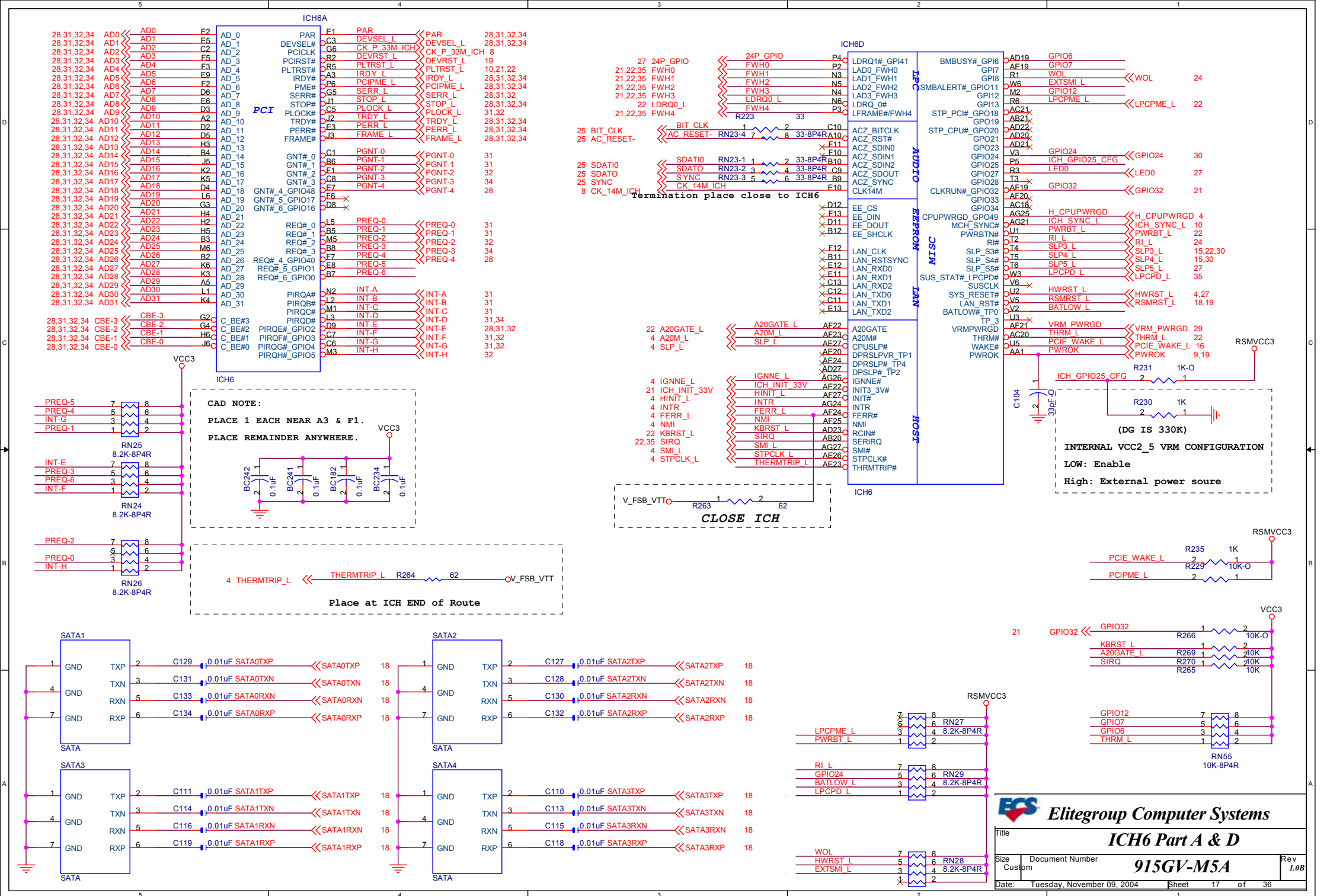


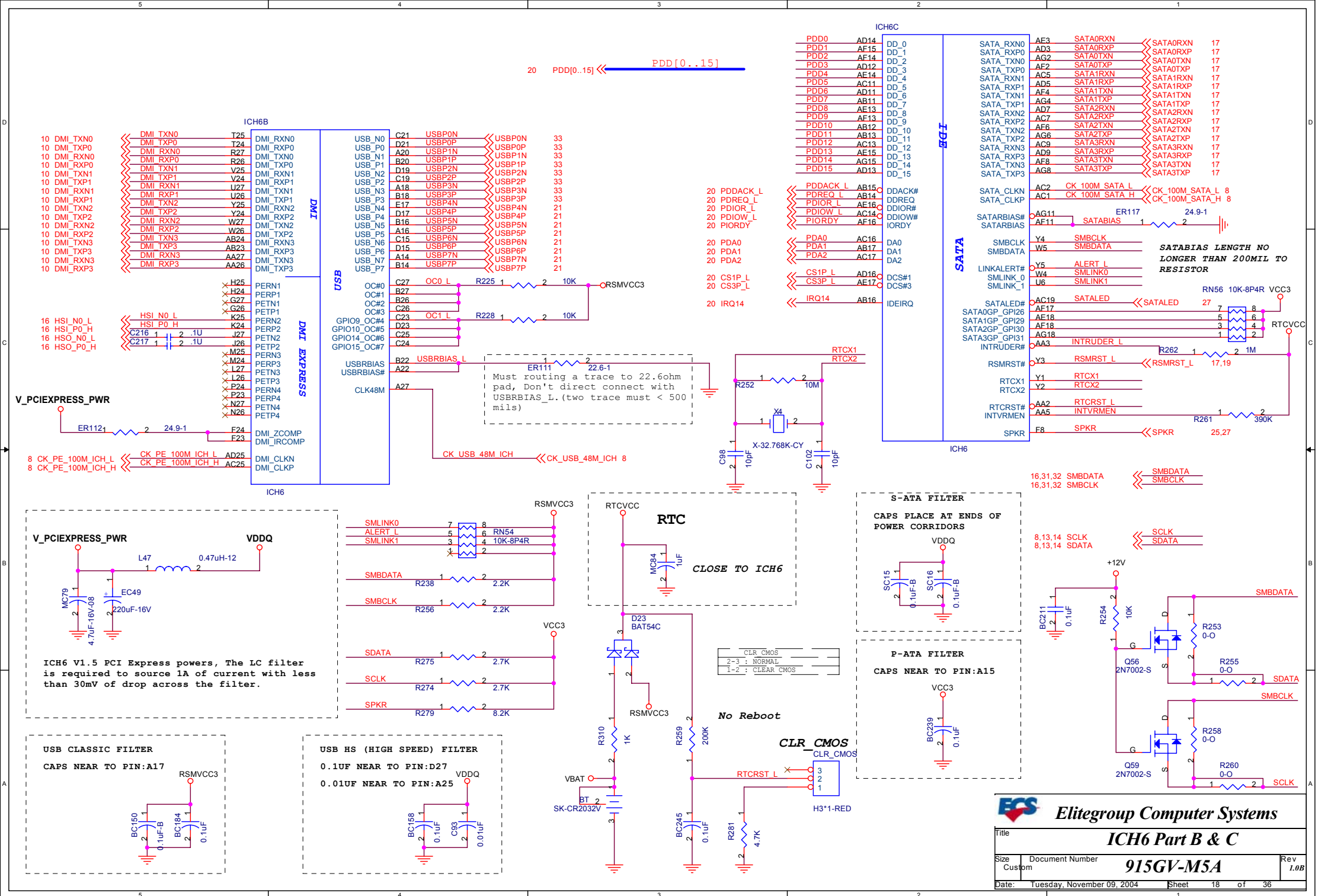
















DATA LINES SHOULD BE MATCHED TO STROBES ( XDIOR\_L, XIORDY\_L) WITHIN +/- 250 MIL.  
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.

# USB PORT INTERFACE

**100 Mils Width**

**USB1:**  
High:XXX Install  
Low:XXX

**USB2:**  
High:1394 Install  
Low:1394 xxx

**GPIO1:**  
High:Suspend xxx  
Low:suspend install

**GPIO2:**  
High:3-COM Lan Install  
Low:Realtek PCI Lan install

**GPIO3:**  
High:3-COM Lan Install  
Low:Realtek PCI Lan install

**GPIO4:**  
High:3-COM Lan Install  
Low:Realtek PCI Lan install

**BIOS\_WP**  
1-2:Flash Write Unprotect  
2-3:Flash Write Protect

**PLCC-32PBR**

**2N3904S**

**Elitegroup Computer Systems**

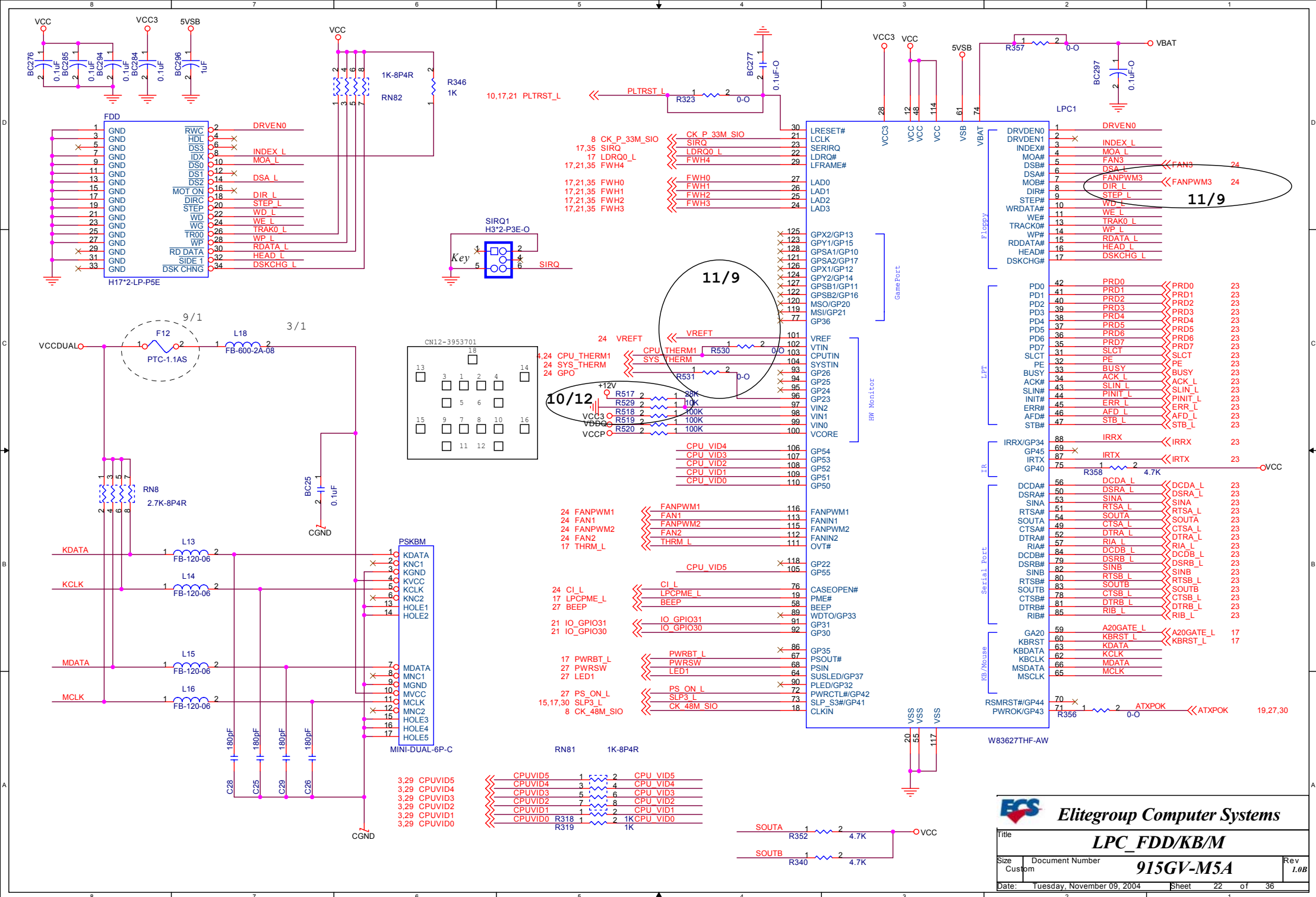
**USB/FWH**

**915GV-M5A**

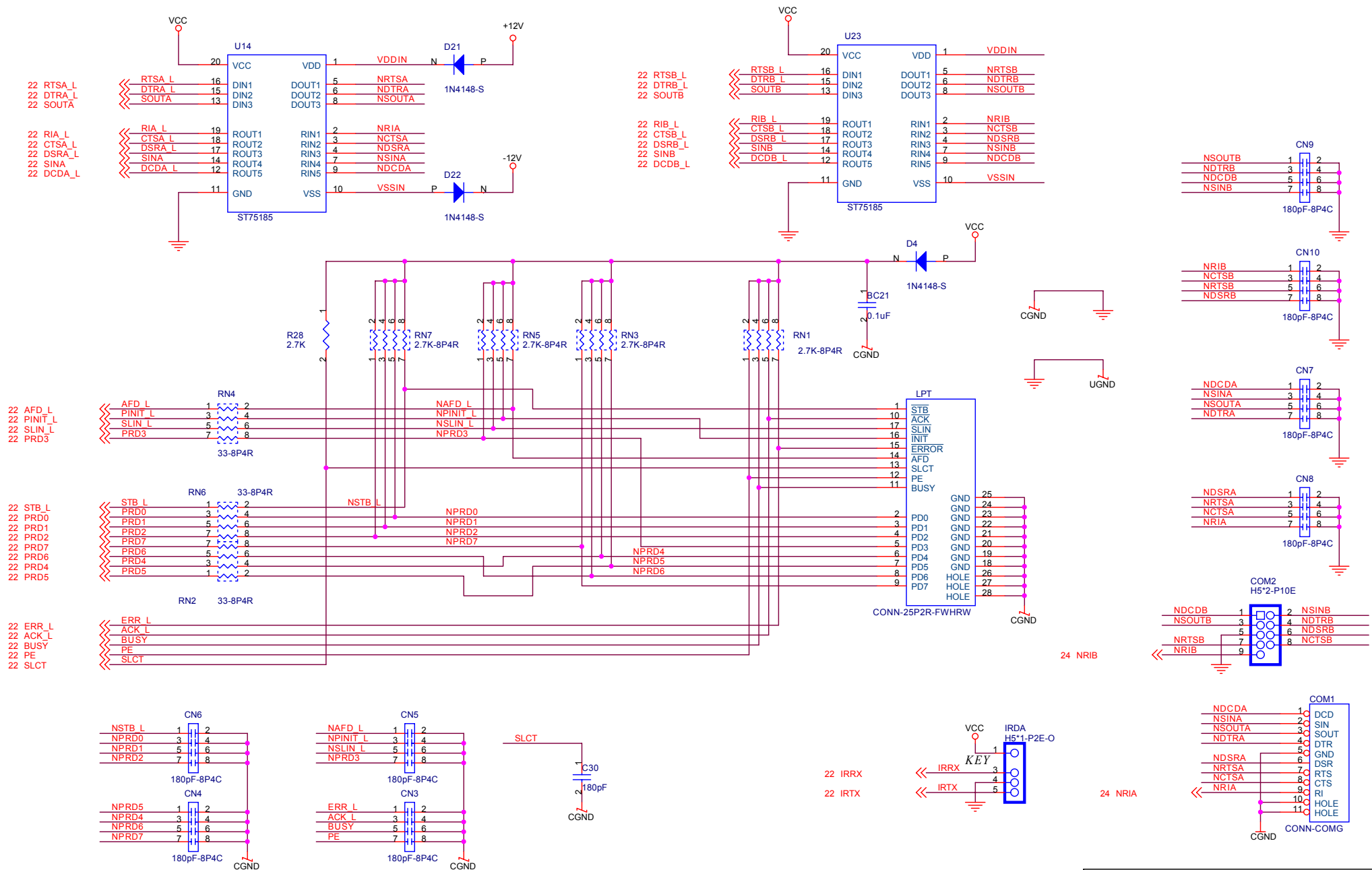
**Rev 1.0B**

**Date: Tuesday, November 09, 2004**

**Sheet 21 of 36**

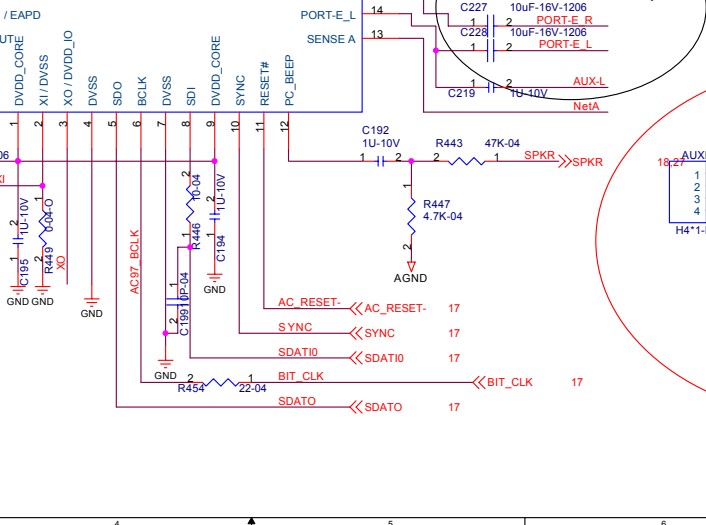
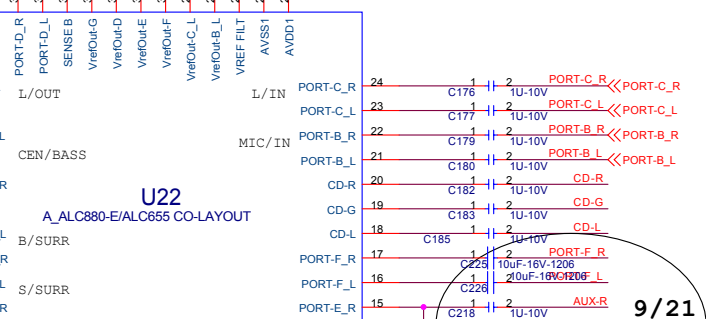
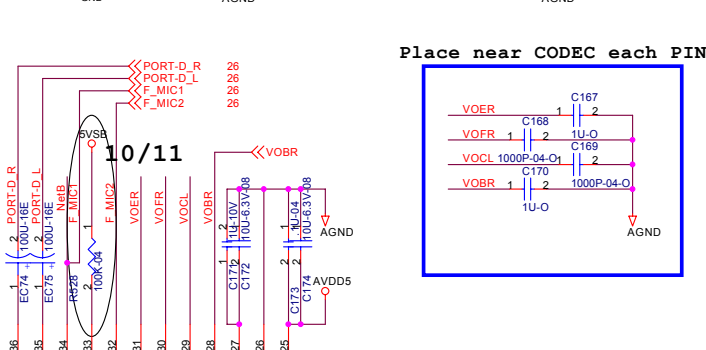
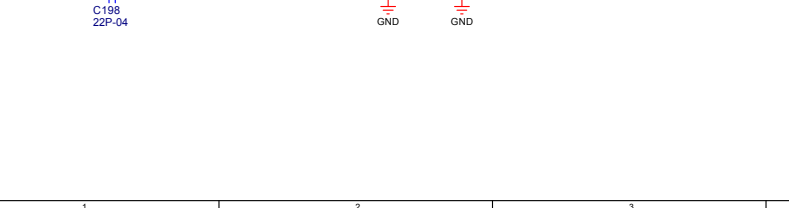
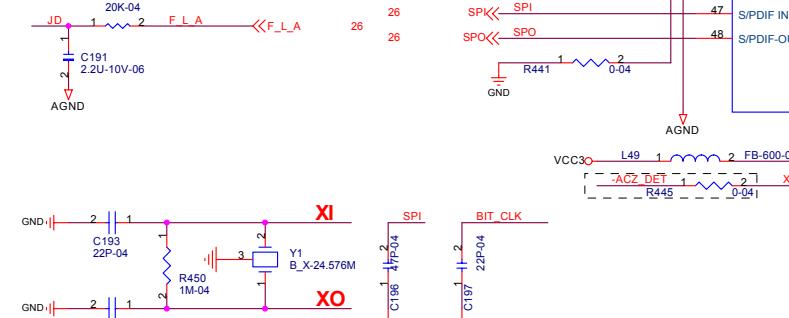
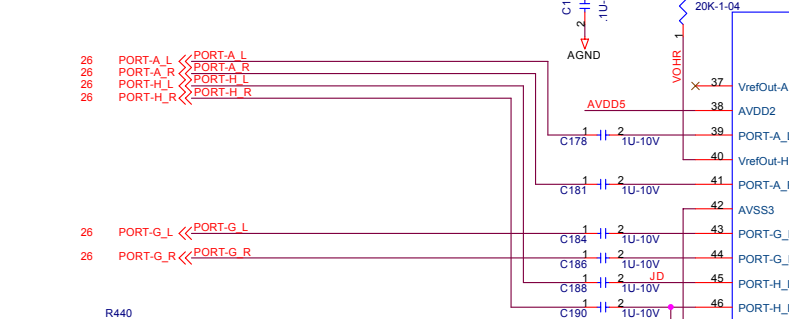




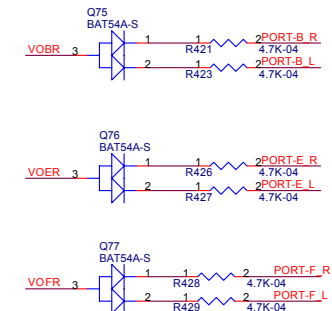




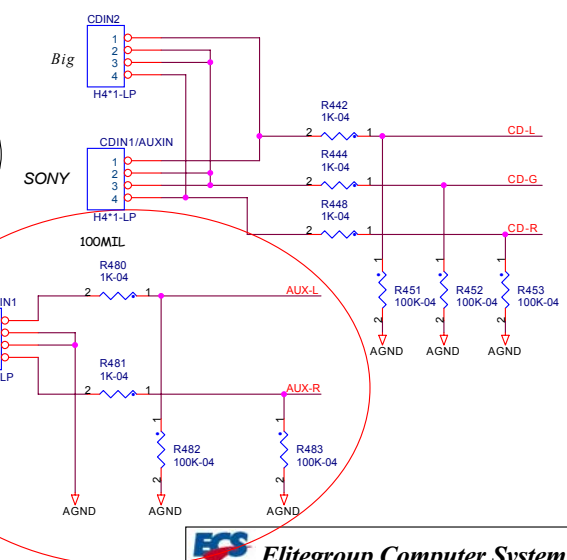
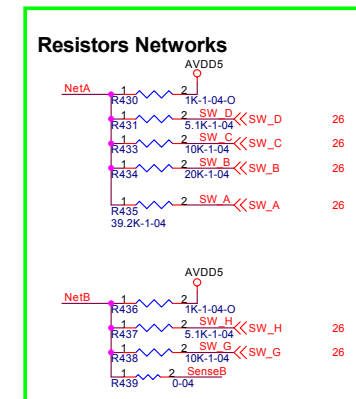




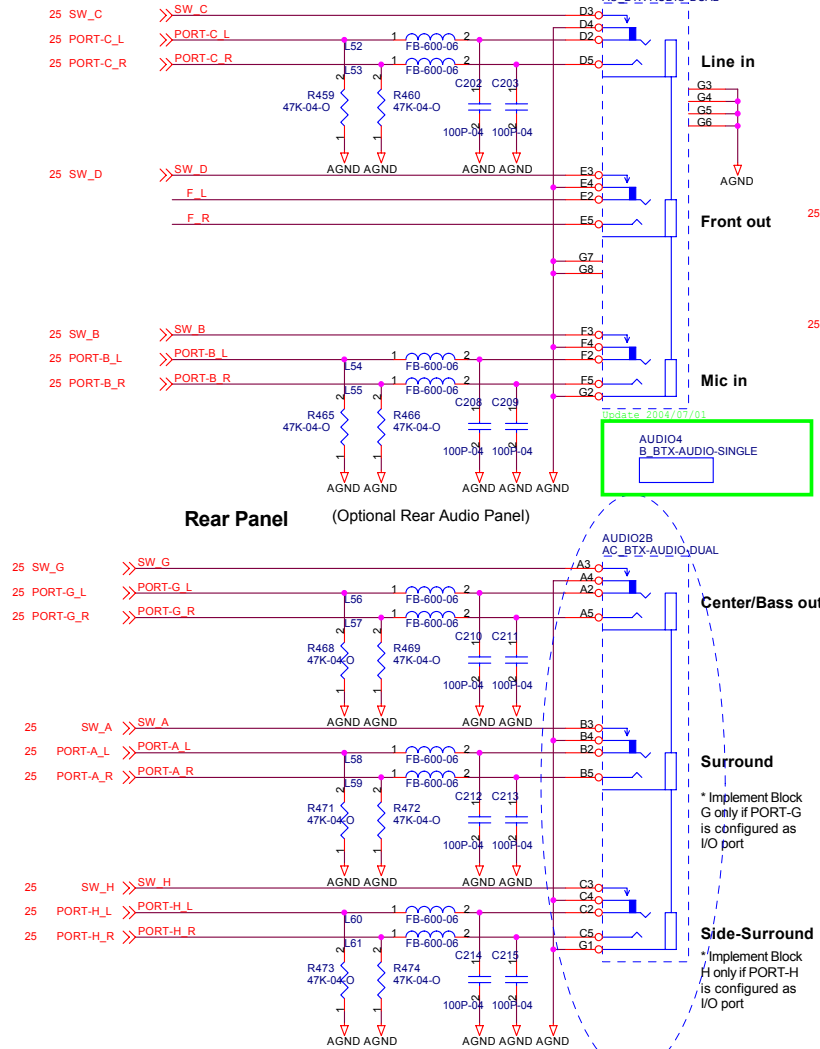
For CMI9880



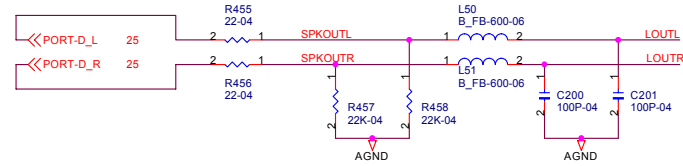
Place near Chip ( U23 )



# Rear Panel Onboard Analog I/O



The schematic should consist with PINs define of I/O connector.

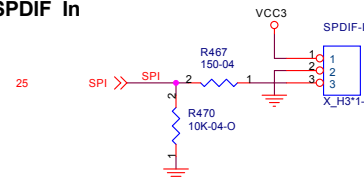


25 F\_MIC1

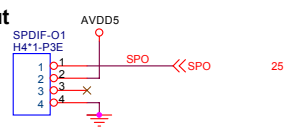
25 F\_MIC2

## SPDIF I/O

### SPDIF In



### SPDIF Out



9/21

ALC880

ALC655

Line in

Front out

Mic in

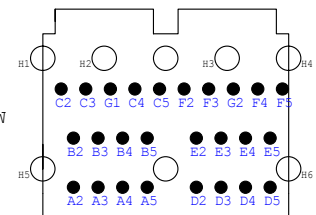
Center/Bass out

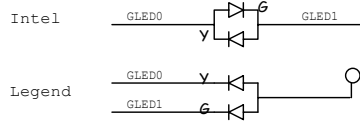
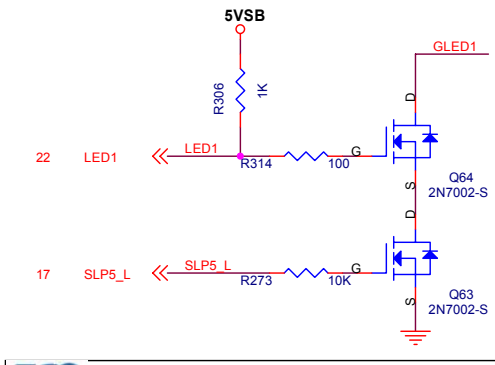
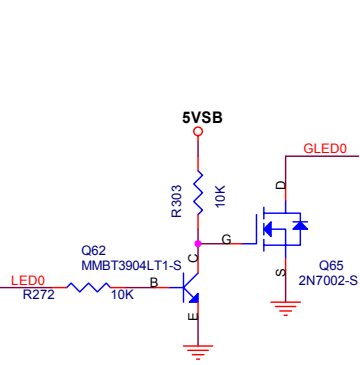
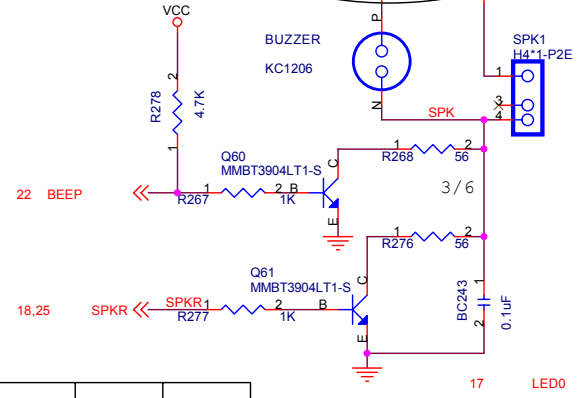
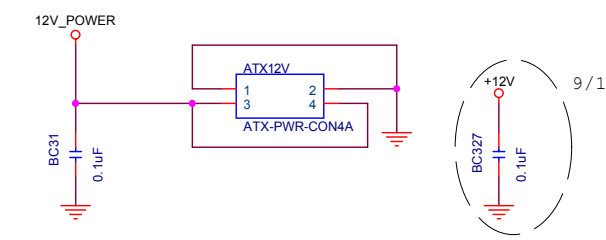
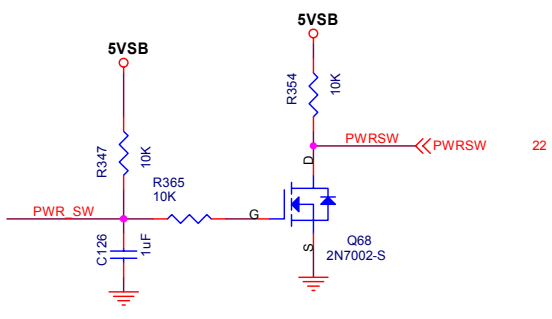
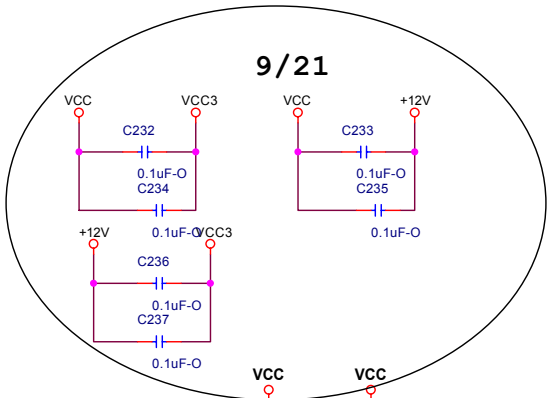
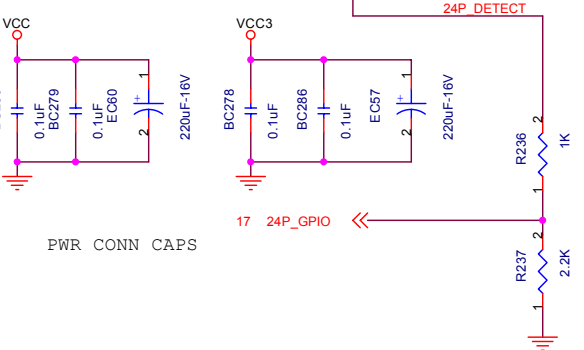
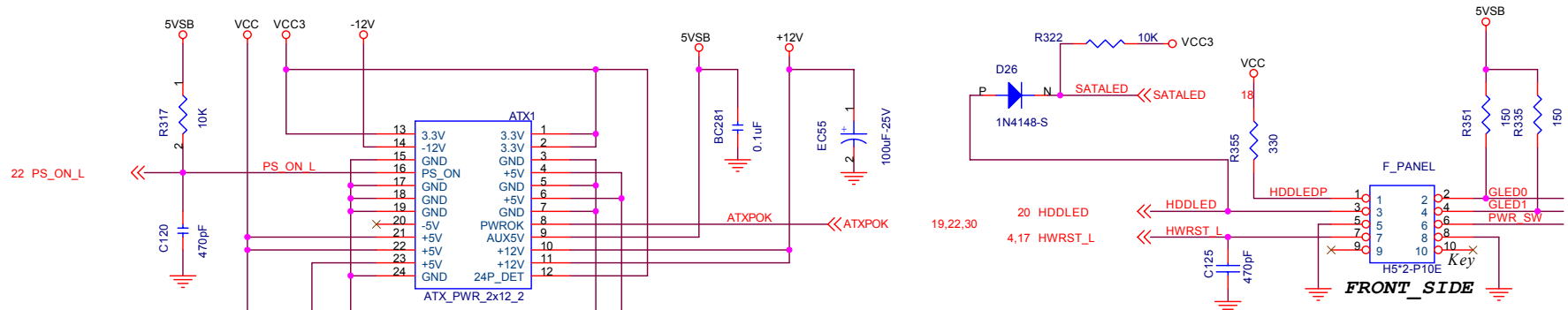
Back-Surround

Side-Surround

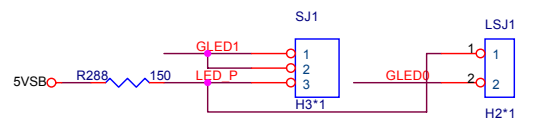
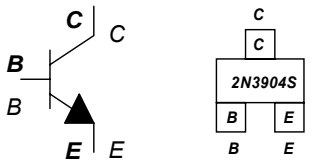
FRONT VIEW

TOP VIEW





	S0	S1	S3	S4,S5
PANEL1 (4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1 (3,5,7)	Green	G-blinking	G-blinking	Dark
LSJ1 (1,2)	Dark	Dark	Light	Dark
SJ1 (1,3) (2,3)	Light	Blinking	Blinking	Dark
GLED0	HIGH	HIGH	LOW	HIGH
GLED1	LOW	SWITCH	SWITCH	HIGH

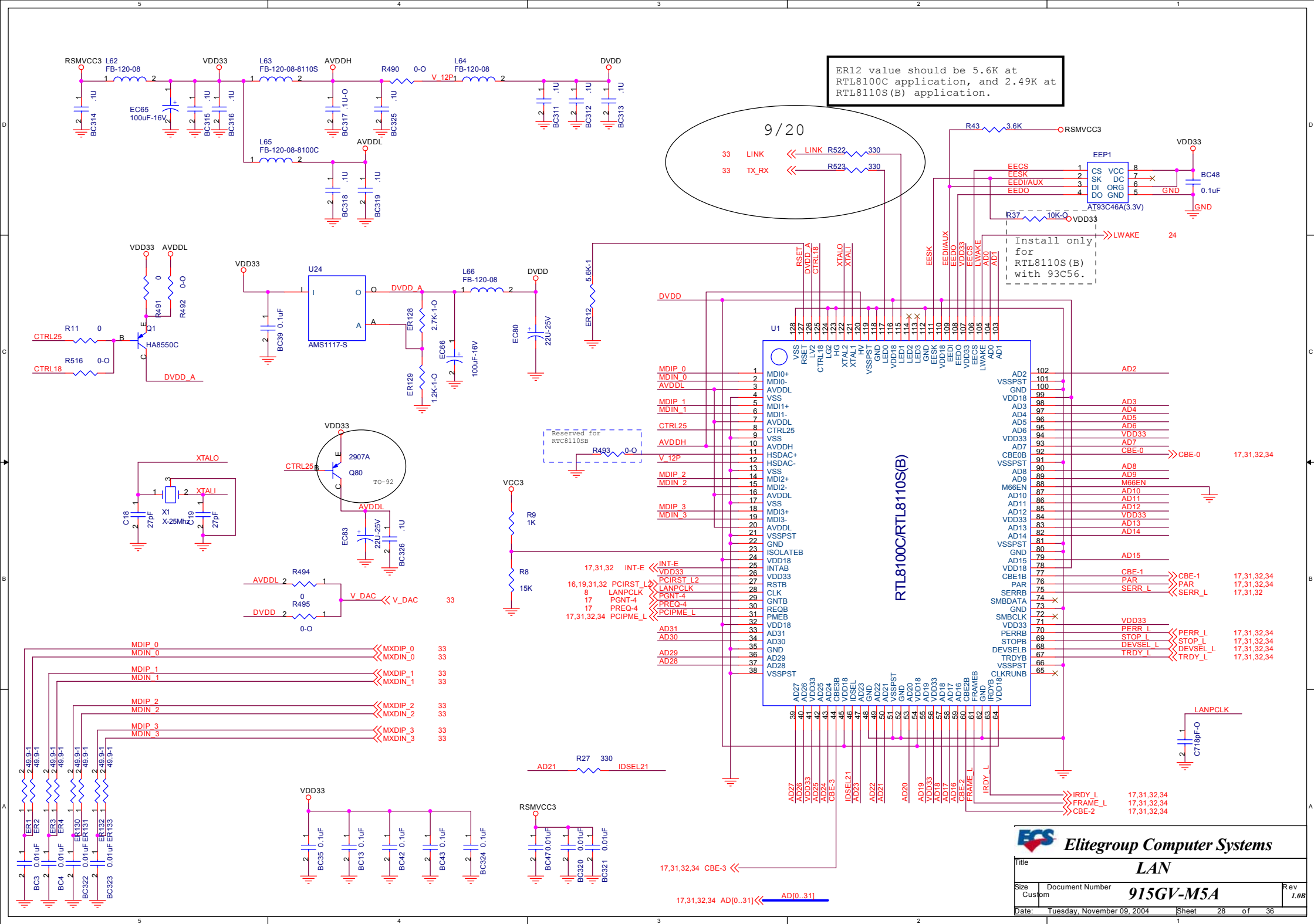


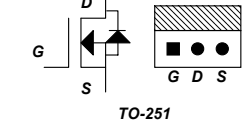
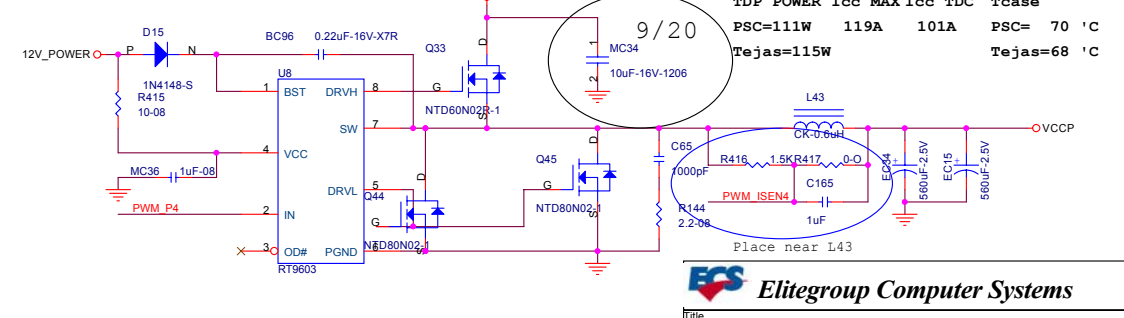
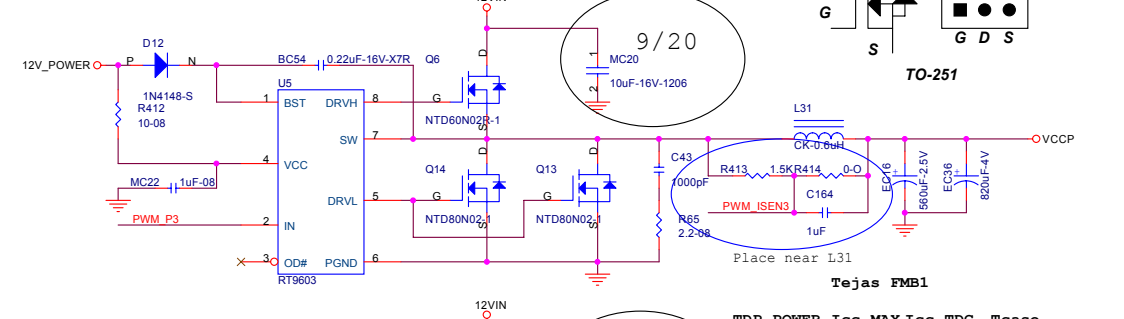
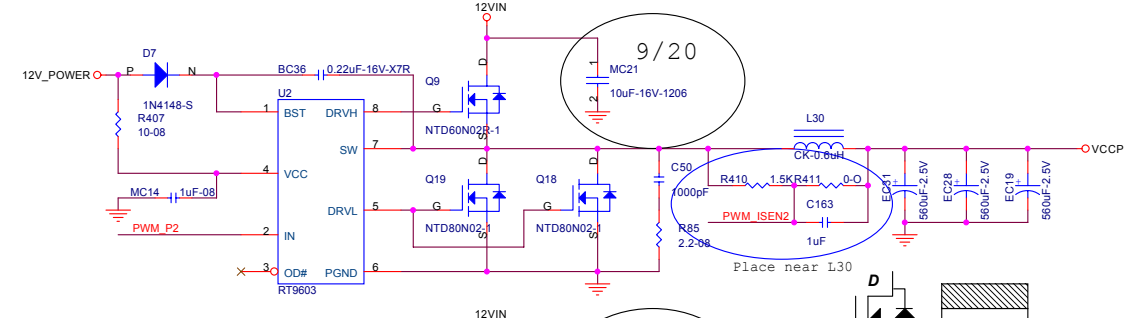
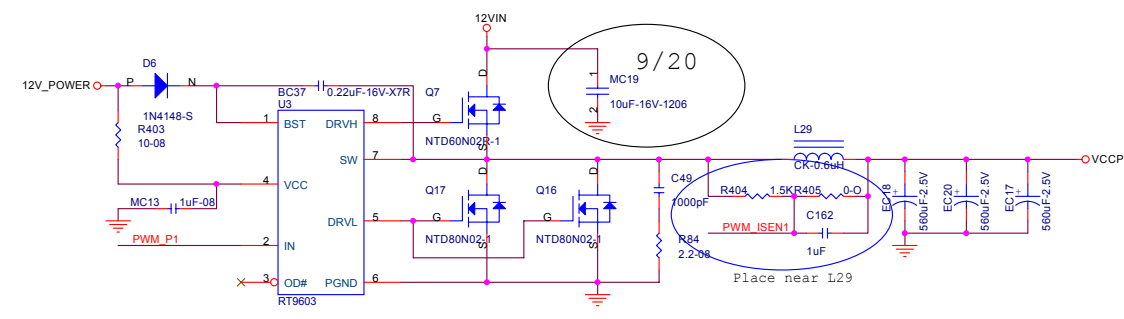
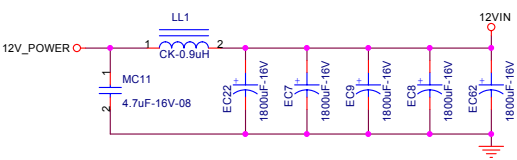
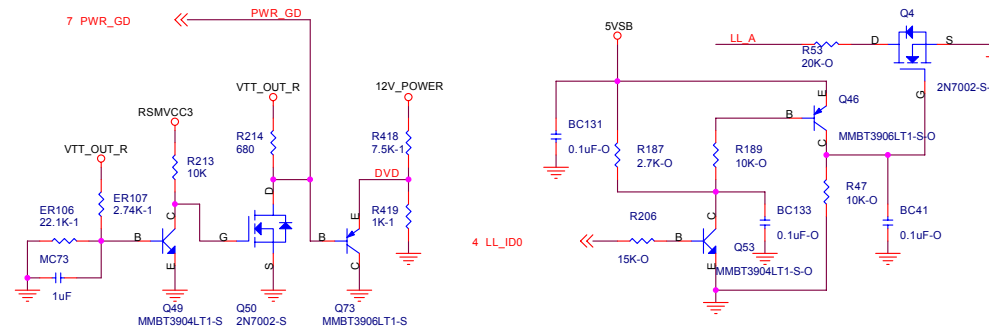
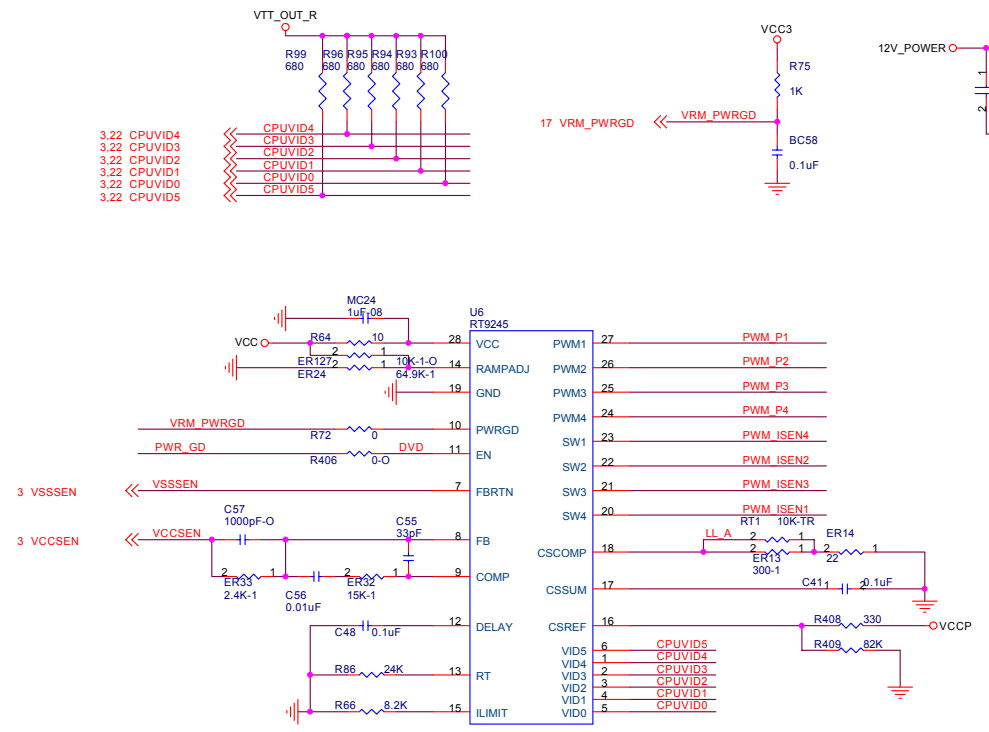
**Elitegroup Computer Systems**

Title: **ATX Power & Front Panel**

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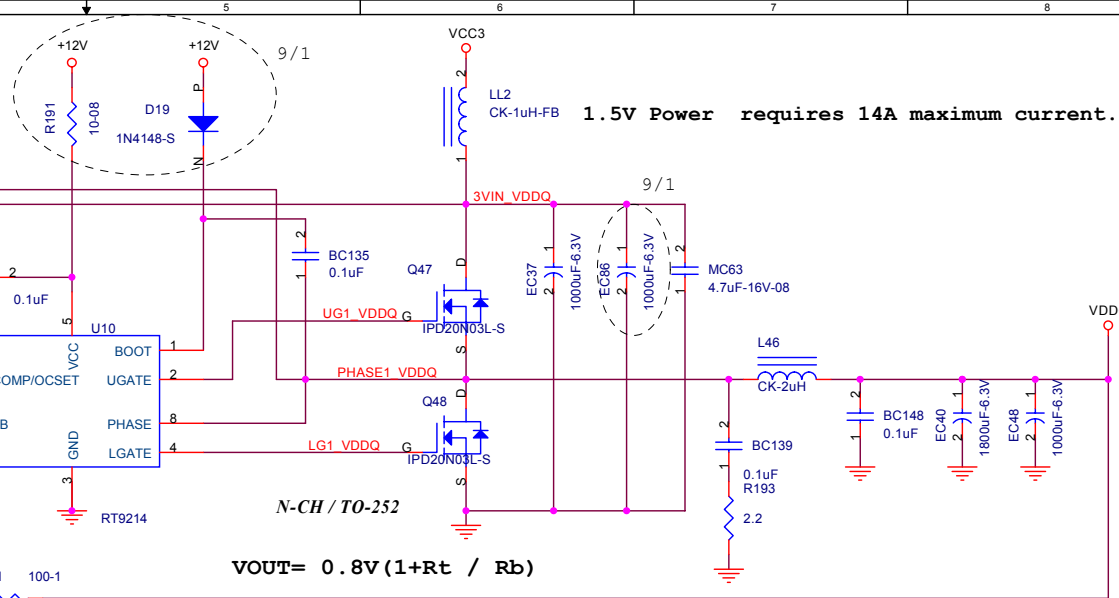
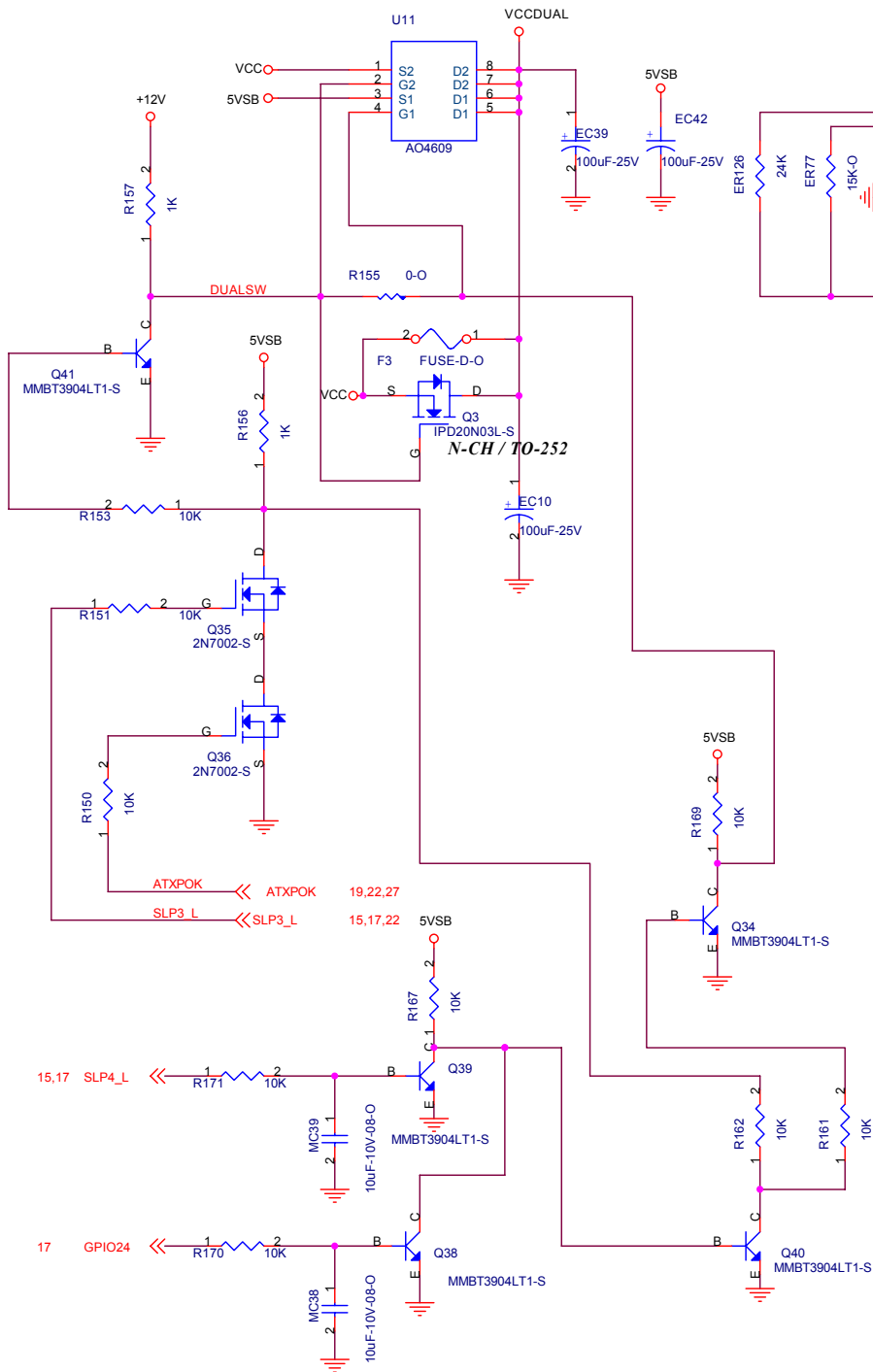




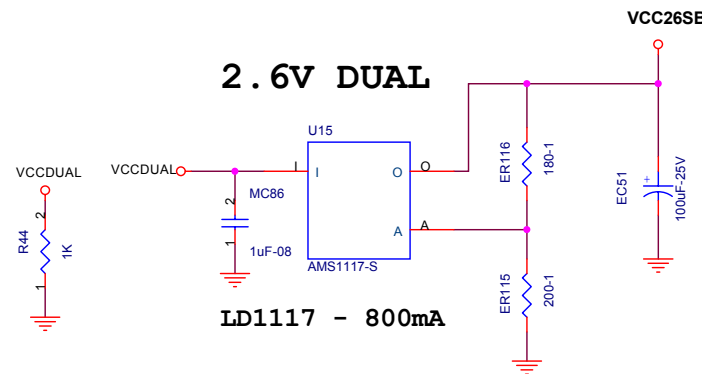
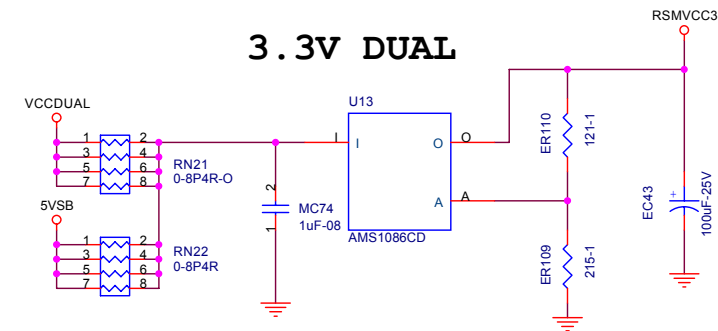
**Tejas FMB1**

TDP	Power	Icc	MAX Icc	TDC	Tcase
PSC=111W	119A	101A	PSC=70 °C		
Tejas=115W			Tejas=68 °C		

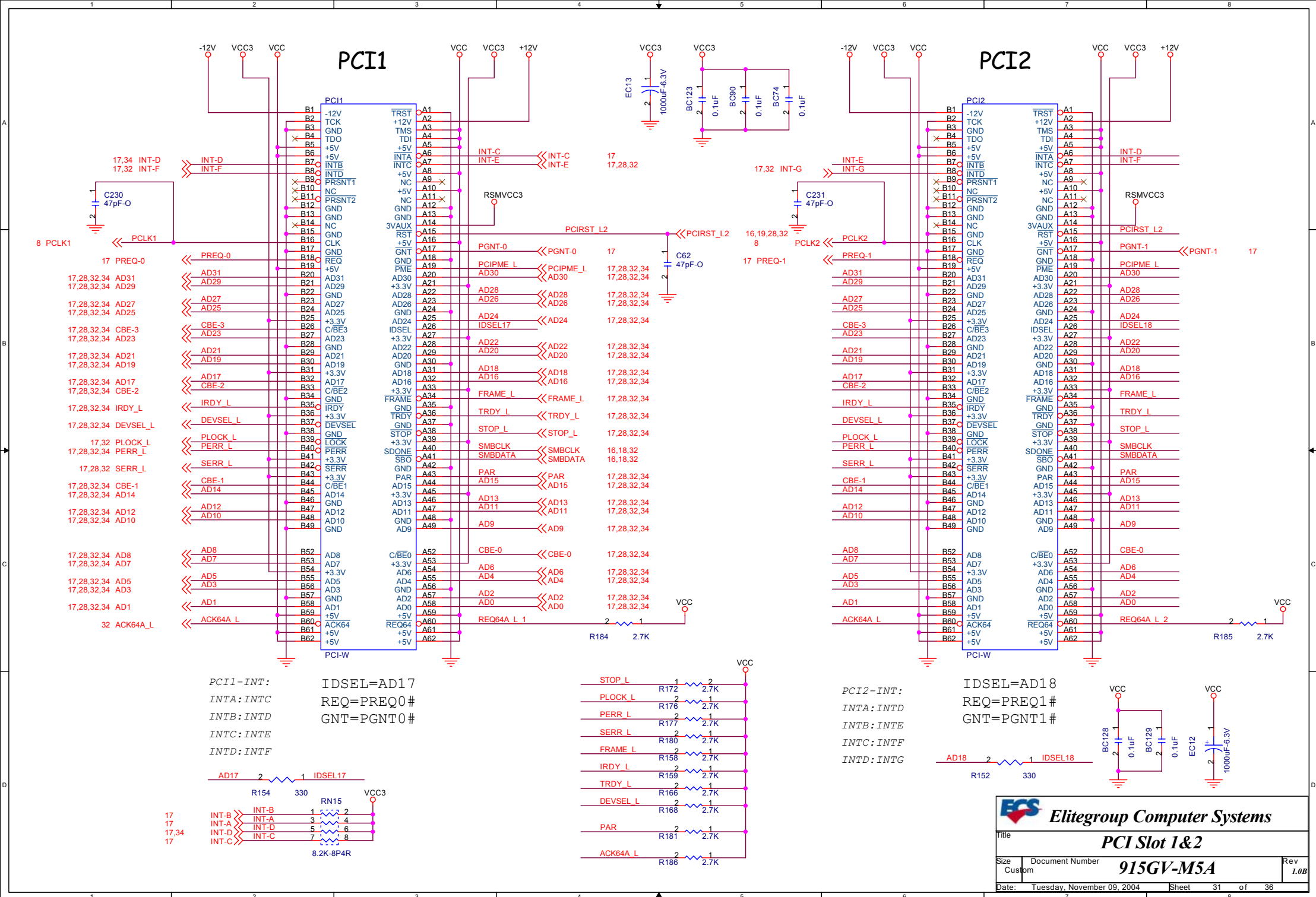
DUALSW << DUALSW 15



Signal Mode	GPIO24	VCCDUAL
S4/S5	0	0 (No Power)
S4/S5	1	1 (5VSB)

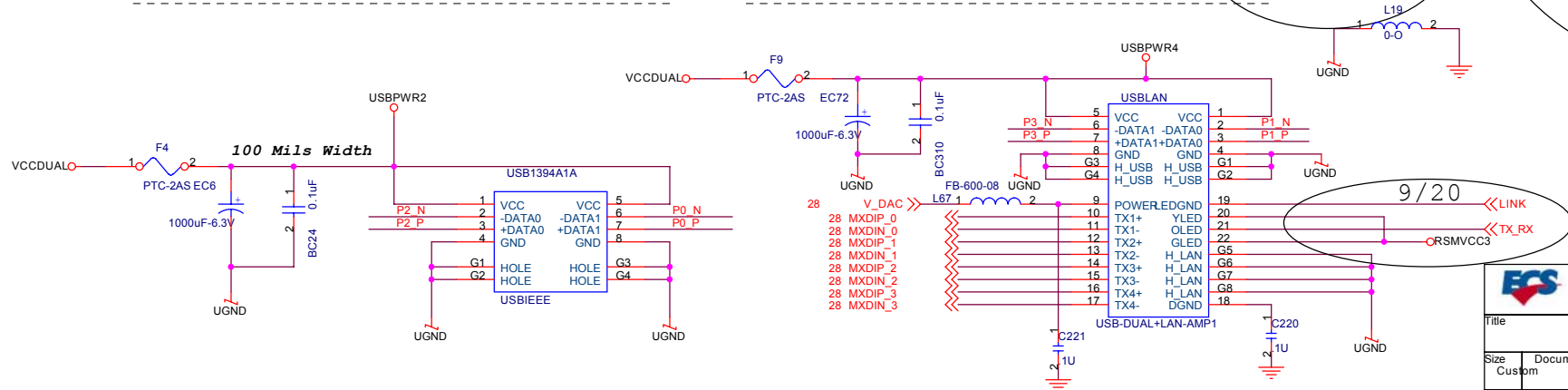
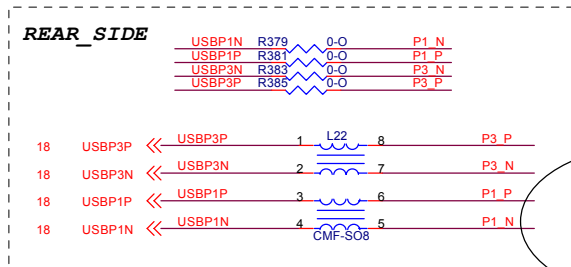
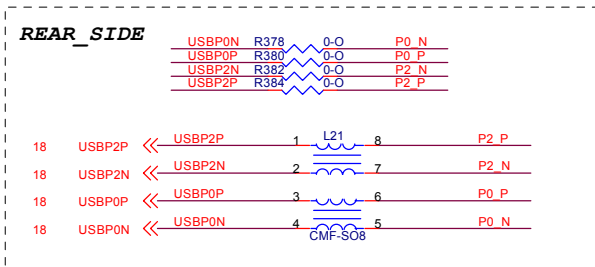
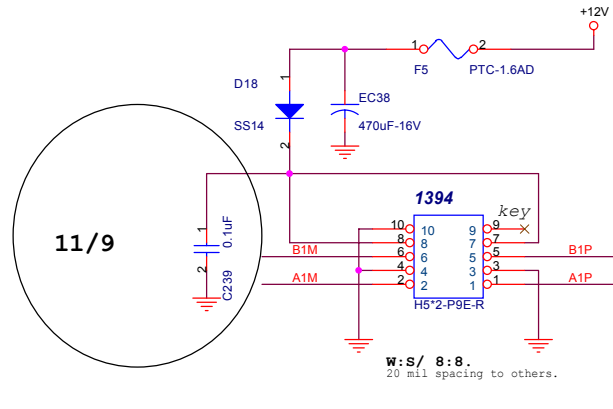
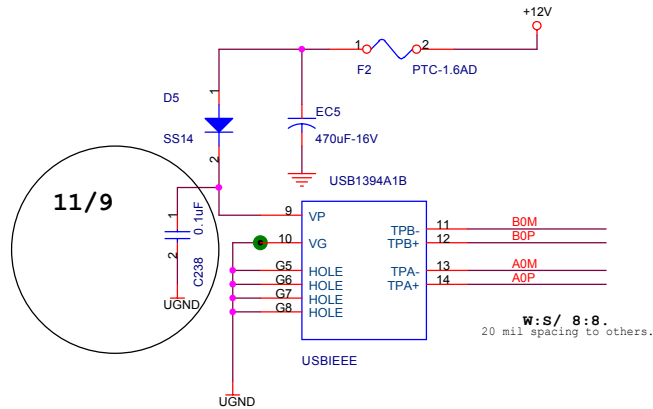
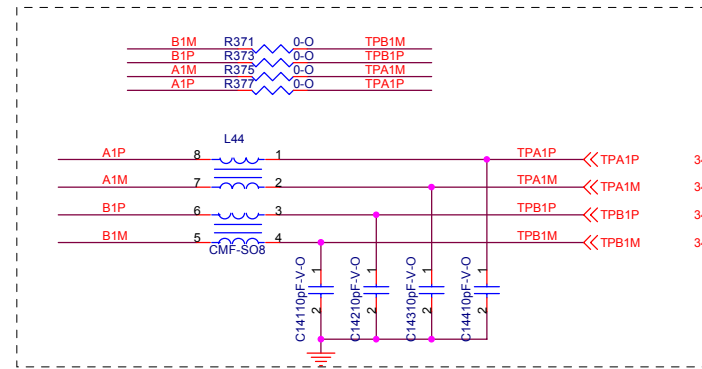
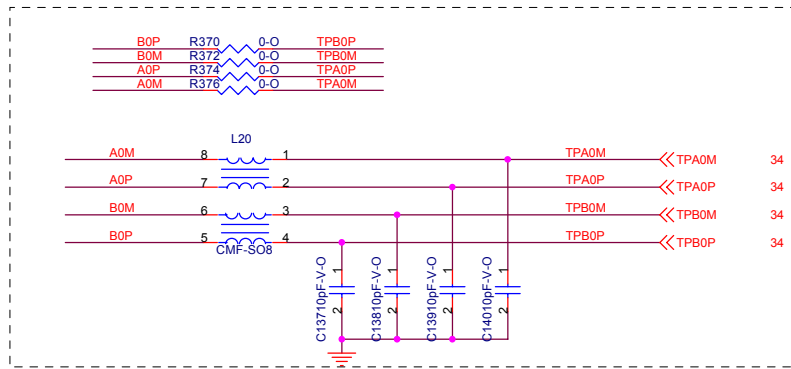


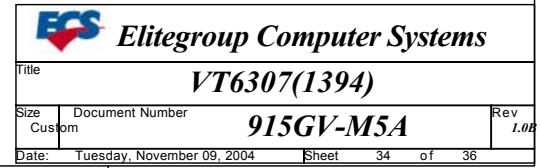
VCC26SB needs supply 570mA of current.



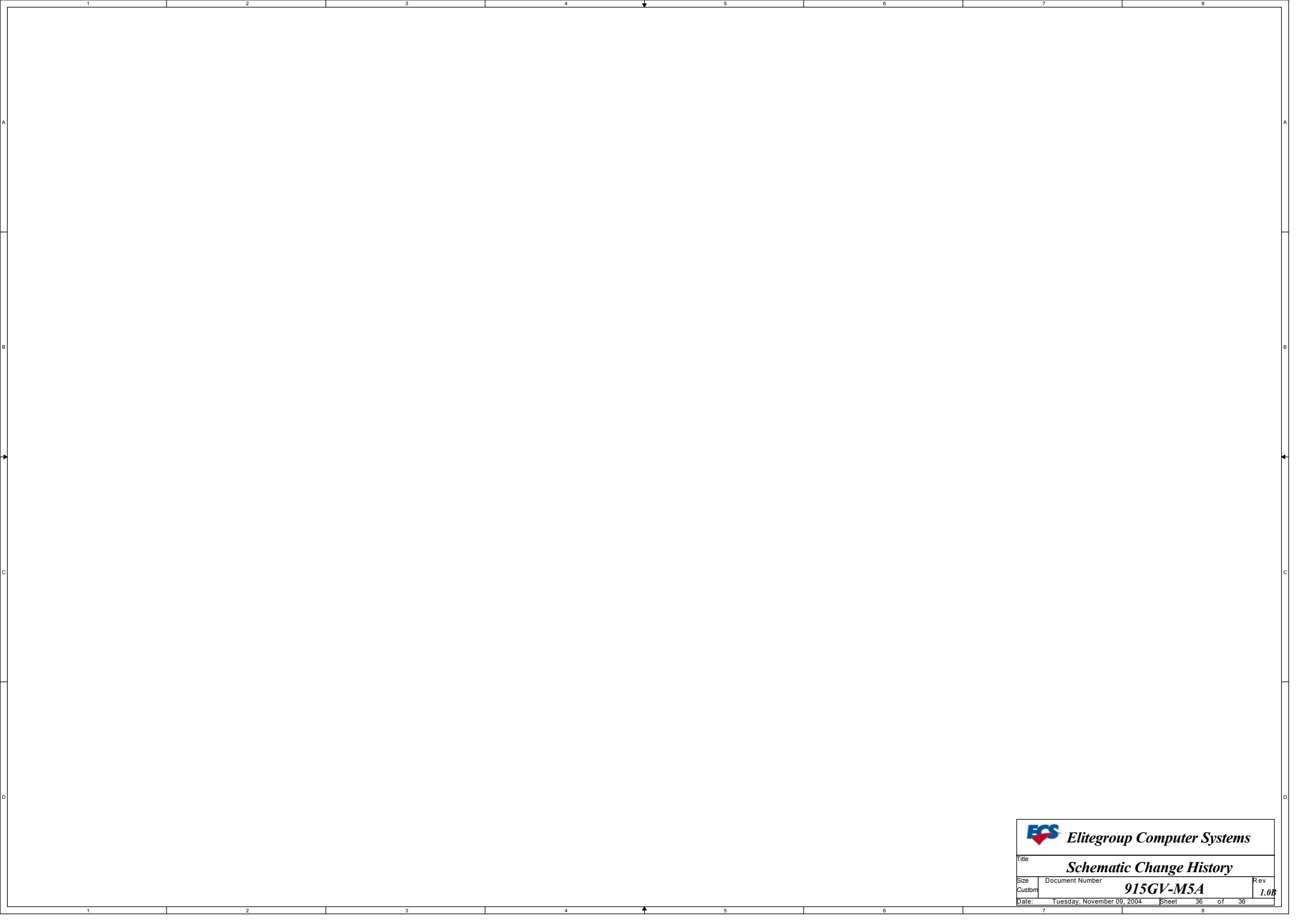













 <b>Elitegroup Computer Systems</b>		
Title <b><i>Schematic Change History</i></b>		
Size Custom	Document Number <b>915GV-M5A</b>	Rev <b>1.0B</b>
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